A LOW-NOISE CMOS INTERFACE FOR CAPACITIVE MICROACCELEROMETERS

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A LOW-NOISE CMOS INTERFACE FOR CAPACITIVE MICROACCELEROMETERS

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To

MY MOTHER XIAO ZHENG

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SUMMARY

In the recent years, there has been increasing demand for low-cost and small-size high-performance MEMS accelerometers with micro-gravity resolution and large dynamic range at very low frequencies. These high-performance accelerometers are applied in GPS-augmented inertial navigation and target monitoring of aircrafts, space station, robotics, land vehicle, train and railway technology, and in wind turbines in natural green energy.

This dissertation presents the design and development of a mixed-signal, low-noise, and fourth-order sigma-delta interface circuit for the MEMS capacitive micro-gravity accelerometer. A fully-differential switched-capacitor (SC) amplifier architecture is developed with the low-frequency noise reduction through the integration of chopper-stabilization technique with lateral BJT at input stage. The effectiveness of different noise reduction techniques is also compared and verified. The application of fourth-order SC sigma-delta modulation concept to the inertial-grade accelerometer is to achieve the benefits of the digitization of the accelerometer output without compromising the resolution of the analog front-end. This open-loop interface provides 1-bit digital output stream and has the versatility of interfacing sensors with different sensitivities while maintaining minimum power dissipation and maximum dynamic range. The micromechanical accelerometers are fabricated in thick silicon-on-insulator (SOI) substrates. The accelerometer operates in air and is designed for non-peaking response with a bandwidth of 500 Hz.

CHAPTER 1

INTRODUCTION

1.1 The Problem

The microelectromechanical system (MEMS) accelerometer has evolved to serve a wide range of applications, such as automotive safety and ride control, inertial navigation, guidance, and motion detection. Though MEMS sensors are commercially available, there are no high-performance, micro-machined accelerometers with a large enough dynamic range to sense low gravity (low-g). Recent advances in micromachining technologies over the past decades have provided a miniaturized, silicon alternative single-axis accelerometer with potentially comparable performance levels. This provides the system designer with an option to strive for a high-performance accelerometer to meet demanding needs.

This research concerns the problem of the reduction of the flicker noise at near-DC frequency range in electronic circuit to interface the MEMS capacitive accelerometer device. The resolution and DR are typically limited by the flicker or 1/f noise of the input transistors at the interface. A new method is developed to prove the effectiveness of the flicker noise reduction made with chopper stabilization technique in CMOS. Before the integration of the lateral BJT into the op amp used in the interface circuit, certain a priori information must be known about it in order to fully take advantage for its effect on the noise reduction. The required lateral BJT (LBJT) information is specified and a method for customized the LBJT is described.

An important consideration in the experimental implementation of high-performance accelerometer interface scheme is that of flicker noise interface reduction at near-DC frequency range. This problem is discussed for the chopper stabilization techniques with custom lateral BJT in CMOS implementation. Switched-capacitor amplifier/scheme/methods are developed. The method is verified experimentally by the measured low-noise power spectral density at the interface outputs to determine noise reduction effectiveness of the interface system. The main goal in applying the sigma-delta modulation concept to inertial sensors is to achieve the benefits of the digitization of the accelerometer output without compromising the resolution of the analog front-end.

1.2 Origin and History of the Problem

An accelerometer is a MEMS device that is used to measure acceleration forces. The traditional applications include vibration measurement, earthquake detection and seismic applications. One of the most common uses for MEMS accelerometers is in airbag deployment systems for automobiles [1-2]. The widespread use of accelerometers in the automotive industry has dramatically reduced their cost. In the present market, single-axis, dual-axis, and three-axis models are commonly available. The performance of micromachined accelerometers has been dramatically improved since the first microaccelerometer was introduced.

Displacement accelerometers measure the displacement of a suspended proof-mass in response to an input acceleration. In [1-2] the authors compare various techniques for measuring accelerometer displacement. These methods include electron tunneling, piezoresistive sensing, piezoelectric sensing, and capacitive sensing. Capacitive position

sensing has a low intrinsic temperature coefficient, high sensitivity, and is easily integrated with CMOS for monolithic sensor-based systems [3]. Capacitive interfaces, however, are particularly sensitive to parasitic capacitance at the system interface, which induces DC offset or excess noise at the system output. For this reason, techniques to reduce the induced noise and DC offset must be developed to meet practical applications.

A functional block diagram of one popular commercial single-axis accelerometer from Analog Devices is shown in Figure 1.1. This figure shows a fully integrated, single-axis capacitive microaccelerometer [4]. This accelerometer operates in an open-loop configuration, providing certain linearity and sensing accuracy without requiring a closed-loop force-feedback scheme. It has a resolution of 110 μg/√Hz with a maximum input of 1.7 g's.

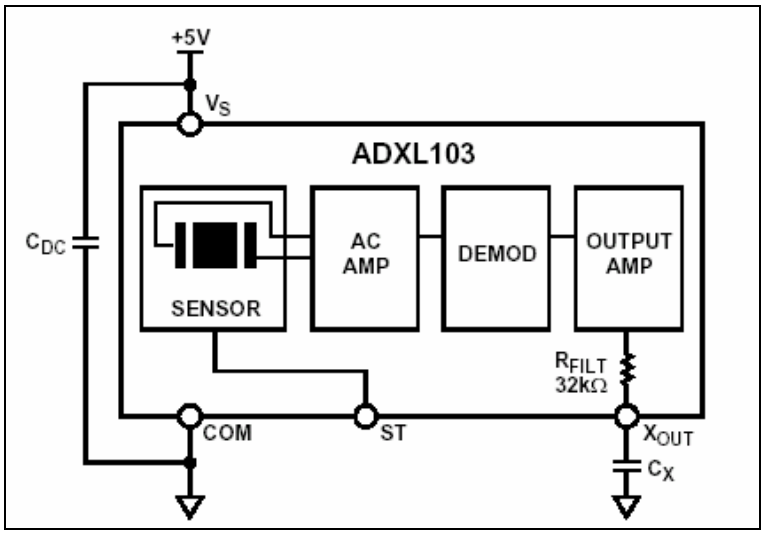


Figure 1.1: Functional block diagram of ADX 013 [4].

A single-axis, high-performance accelerometer that senses low gravity with a low-noise interface was successfully developed in [5]. High quality accelerometers can

be realized in an ultra-small size for large volume production. Conventional systems are bulky, complex, and expensive. Figure 1.2 shows a commercial three-axis accelerometer.

Figure 1.2: A three-axis micro-gravity accelerometer from ZIN Technology [6].

The development of MEMS technology, coupled with the advances of CMOS technology, has demonstrated the feasibility of a sensing accelerometer with a single proof-mass in both open-loop [7] and closed-loop configurations [8]. A closed-loop system implementation has the ability to extend dynamic range, increase linearity, flatten frequency response, and improve cross-axis rejection [9-10].

The noise floor of the electronic interface circuit must be lower than the MEMS accelerometer mechanical noise floor of the device in order to achieve a high resolution. The noise performance of the system determines the minimum detectable acceleration range; therefore, it is the primary research in the past [1-2, 11-12]. In the simplest case of an interface, consisting only of an analog front-end circuit, the resolution is determined primarily by the noise of the switched-capacitor amplifier (capacitance-to-voltage converter), which is the first stage in the signal path. The resolution of the capacitive micro-g accelerometers interfaced with a low-cost CMOS IC is typically limited by the

flicker or 1/f noise of the input transistors at very low frequencies. In semiconductor transistor, the flicker noise is generated by tunneling effects in the surface oxide layer of the material. This type of noise seems to be a systematic effect inherent in electrical conduction, resulting from a variety of effects, such as impurities in a conductive channel, generation and recombination noise in a transistor due to the channel current. Techniques to reduce the noise floor and 1/f flicker noise in the low-frequency range had been implemented [2, 5, 13-15]. Although there have been a few reports of micro-g resolution at input frequencies higher than 10 Hz, achieving near DC micro-g resolution has proven to be difficult with small-sized MEMS sensors suitable for consumer applications [5, 16-18].

In the recent years, there has been increasing demand for low-cost and small-size high-performance MEMS accelerometers with micro-gravity resolution and large dynamic range at very low frequencies. These high-performance accelerometers are not only used in GPS-augmented inertial navigation and target monitoring of aircrafts, helicopters, space station, tactical missiles, wind tunnel and more in military/aerospace application [11], but also in robotics, land vehicle, train and railway technology, and large machinery monitoring in civic industries, such as guidance and monitoring of pipeline drilling in oil-drill platform, wind turbines in natural green energy [12, 19-25].
As shown in Figure 1.3, there has been no investigation of micro-gravity MEMS accelerometer at near-DC frequency range in the past. In response to such performance needs, there is a demand to develop a large systems with distributed high reliability and low-power microaccelerometer systems. Our group has been working on a project to

explore accuracy and resolution limits of capacitive microaccelerometers with a goal of achieving micro-gravity resolution in an integrated cost-effective implementation.

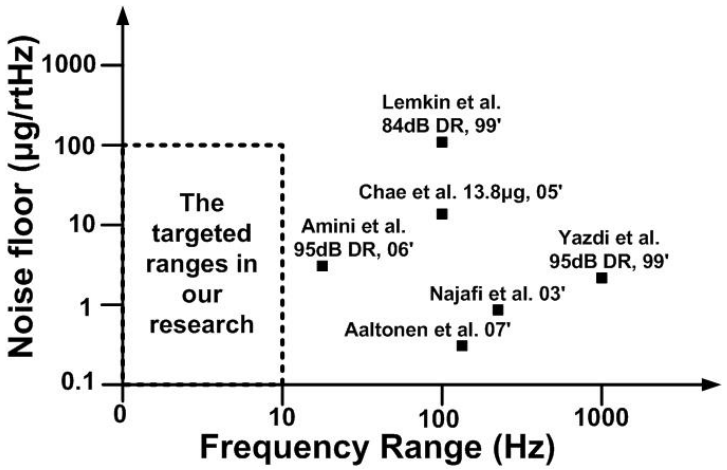


Figure 1.3: Prior research work at low frequency range.

The performance level of open-loop capacitive micro-accelerometers is limited in terms of linearity, dynamic range, and bandwidth when large background accelerations exist. For a linear operation, the displacement of the proof-mass should be so small that the secondary effect of air-damping (D), tether stiffness (K), and electrostatic forces applied by readout electronics are negligible and do not degrade the overall performance [5]. A large input acceleration causes a large displacement that can push the accelerometer into the nonlinear operation region. Therefore, dynamic range is limited for an open-loop system.

For a closed-loop accelerometer system, the force balancing of the proof-mass is attained by enclosing the proof-mass in a negative feedback loop. The feedback loop measures deviations of the proof-mass from its neutral position and applies a force to the same proof-mass to keep it centered. The accelerometer output is taken as the force

needed to keep the neutral position. Because the output is dependent only on the feedback force, the device is insensitive to first-order variations in the mechanical spring constant; i.e., the effective spring constant is changed. By maintaining the small displacement of the proof-mass, nonlinearities from the mechanical system and electronics interface are minimized. In addition, the bandwidth of the closed-loop system can be extended beyond the natural frequency of the open-loop system [12].

Nevertheless, closed-loop force balancing is not desirable for low-cost and low-power applications. In these applications, the added complexity, die size, power consumption, and manufacturing cost are often the limiting factors. Also, the input referred noise of the closed-loop system is relatively high. High-performance micro-machined inertial sensors with micro-gram resolution usually take advantage of closed loop control to increase their dynamic range, linearity and bandwidth. The general system diagram of a closed-loop system is shown in Figure 1.4:

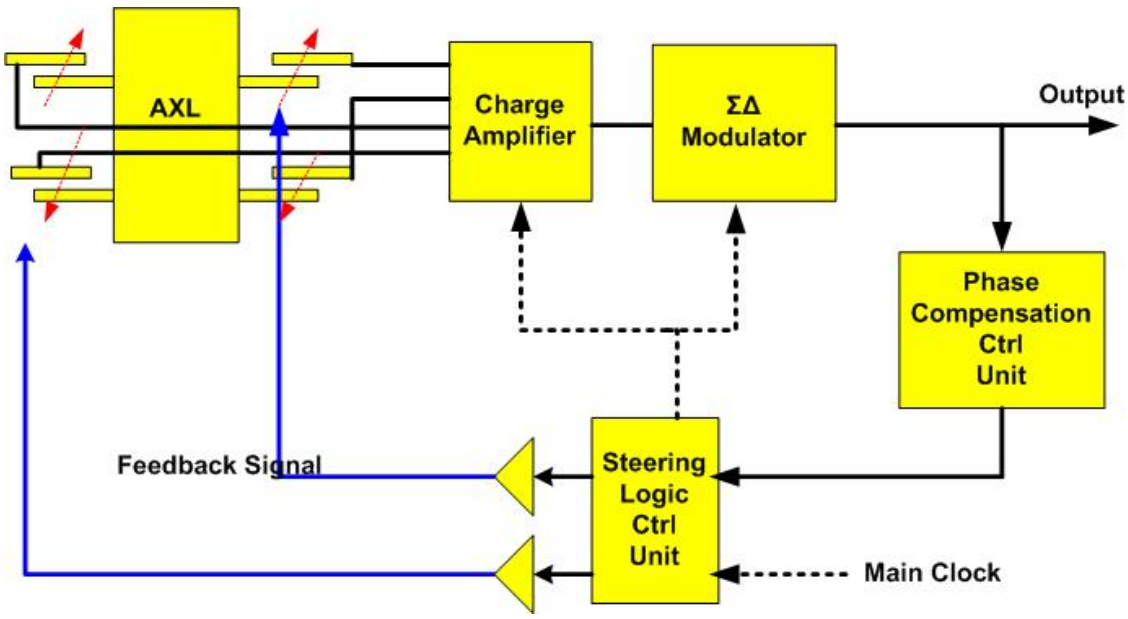


Figure 1.4: A closed-loop, single-axis accelerometer function diagram.

Figure 1.4 shows a digital closed-loop accelerometer system consisting of:

- the micro-machined sensing element (accelerometer),
- a circuit converting the differential change of capacitance into a voltage,
- a sigma-delta ($\sum\Delta$) modulator to provide the oversampling conversion,
- a phase compensation unit to provide the stability control of the loop, and
- a steering logic circuit to provide all digital clocks and control signals.

For simplicity, the sensing element is depicted as four variable capacitors in four corners of the proof-mass. In this design, only during the sensing phase is the charge amplifier connected to the proof-mass. The output of the charge amplifier is proportional to the differential capacitance change. To avoid the electrostatic pull-in problems of purely analog force feedback control systems. The electrostatic feedback force of the accelerometer is controlled by the high frequency, digital pulse-density-modulated output bit stream of the sigma-delta modulator, Therefore, the closed-loop accelerometer offers the same advantages of an electronic over-sampled sigma-delta data converter, which are: 1) direct digital output, 2) wide dynamic range, 3) extended linearity, and 4) less stringent precision requirements of the circuit blocks.

For closed-loop signal acquisition, processing, and transmission, each unit in a signal processing loop has to be at least as accurate as the whole system. However, a typical ADC limits the overall accuracy and dynamic range in signal processing systems. As a result, to improve the performance of the signal processing systems, the designs of the ADC's have to be improved.

The main goal in applying the sigma-delta modulation concept to inertial sensors is to achieve the benefits of the digitization of the accelerometer output without

compromising the resolution of the analog front-end [12, 26-28]. Therefore, the sigma-delta modulator must be designed such that the quantization error adds a negligible noise penalty. In addition to suppressing of the noise from the quantization, the sigma-delta modulator loop must be compensated appropriately for stability. A notable advantage of the sigma-delta modulator is that it combines low-order integrators and a low-order anti-aliasing filter successfully with oversampling. This oversampling ensures that the out-of-band frequencies that are not completely attenuated by the low-pass filters will not be aliased when sampled by the modulator.

The demand for high-resolution interface circuits compatible with digital processors, in particular, with the availability of low-cost, high speed, high density of VLSI technology, made oversampling data converters very popular in recent years [29-31]. The overall cost of a sigma-delta modulator electronics still remain low cost, comparing to other approaches. All these advantages are achieved by trading-off resolution in time domain with resolution in voltage domain. Oversampling data converters provide high-resolution at the expense of reduced speed and some digital circuitry. A special case of oversampling ADC's, delta-sigma ($\sum\Delta$) ADC, achieves the tradeoff between resolution and speed in an efficient way, and does not suffer from circuit imperfections [32-33].

The electromechanical system formed by the accelerometer and the interface electronic circuitry has a number of non-ideality and non-linearity sources that affect the overall performance. Disadvantages of using sensing element into an electro-mechanical modulator are its equivalent low DC-gain that leads to a lower SQNR [12]. So it is desirable for high-performance inertial sensors to have a quantization noise level at least

one order below both the mechanical noise and electronic noise. For high order electro-mechanical modulator, not only the order and topology of the electronic filters, but also the sensing element determine the quantization noise shaping, which severely degradation compared to the electronic counterpart.

The $\Sigma\Delta$ ADC is probably the most used ADC architecture nowdays. These ADC's fit perfectly on the same chip with digital processors, or at least better than other architectures. They are very versatile, converting from seismic signal in the mili-hertz range up to communication signals reaching into tens of mega-hertz, with resolutions of 10, 16 or 24 bits. Their complexity ranges from the simplest first-order with a single-bit quantizer to cascaded 5th-order with multi-bit quantizer in each loop. Most of the reported designs are based on industry's "trusted solutions" since no accurate analytical model is available for the general use.

The ADC systems can be categorized into two major groups: Nyquist-rate and oversampling converters. While there are many ways of implementing a force-feedback accelerometer closed-loop, a sigma-delta modulator used as an oversampling ADC is particularly attractive because it has a relatively simple structure, provides digital output with a large bandwidth, and is easily implemented in CMOS technologies [10, 29]. Oversampling ADC's can be classified into two main groups: straight-oversampling and noise-shaping ADC's. Straight-oversampling ADC's exploit the fact that the quantization noise is assumed to be uniformly distributed white noise over the entire frequency range. The higher the sampling frequency, the lower the quantization noise power per frequency. On the other hand, the noise-shaping ADC's achieve a more efficient accuracy / speed trade-off by utilizing the noise-shaping concept in addition to oversampling. The noise-

shaping is performed by placing the quantizer in the feedback loop in conjunction with a loop filter to reduce the quantization noise, which is created by converting an analog signal to a digital signal. The noise-shaping ADC employing a coarse quantizer is known as a sigma-delta ADC. Since the spectrum of the processed signal covers only a small fraction of the Nyquist bandwidth, the shaped noise can be filtered outside of the signal bandwidth in the digital domain. Oversampling, noise shaping, and filtering can result in exceptional accuracies. The bandwidth and/or frequency of the processed signal are not very high; however, it is well suited for the accelerometer interface design to achieve a high-resolution accuracy. In state-of-the-art oversampling ADC's, the oversampling ratio typically is between 8 and 256. Oversampling ADC's are based on trading off accuracy in amplitude for accuracy in time [29]. Unlike the Nyquist-rate converters, sampling is not a major problem for oversampling ADC's. Normally, dedicated sample/hold circuits are not required, because sampling is performed inherently by the circuits that perform quantization.

On the other hand, Nyquist-rate ADC's use clock frequencies, which are not very high compared to the frequency of the processed signal. Nyquist-rate ADC's are used to digitize high-frequency and/or high-bandwidth signals. Since the frequency and/or bandwidth of the processed signals are very high already, oversampling is often impractical. This research concentrates on oversampling ADC's, thus Nyquist-rate ADC's will not be discussed further.

In order to achieve a large signal-to-noise-ratio (SNR) and high resolution in one sigma-delta ADC circuit, adopting a higher-order structure is inevitable. In reality, a sigma-delta ADC is a highly nonlinear circuit. When more than two integrators are

cascaded in the sigma-delta modulator loop, it becomes prone to instability when the modulator is excited by a large input signal.

The most commonly used modulator structures are the distributed feedback (DFB) and distributed feed-forward (DFF) type modulators. Multiple methodologies have been developed in the past to improve the sigma-delta modulator's stability condition. The mixed structure combining DFB and DFF is based on cascaded integrators with feedback branches to position the poles and feed-forward branches to position the zeros. It provides the proper SNR performance and flexible stability control through these coefficients. However, these structures are complicated. The exact coefficient positioning is difficult to maintain in the circuit implementation.

An alternative method of implementing a higher-order sigma-delta modulator is to cascade multiple lower-order stages in such a way that each stage processes the quantization noise of the previous stages. It is commonly called the multi-stage (MASH) modulator. The quantization noise of all stages, except the last stage, is removed and the last stage quantization noise is high-pass filtered by the noise transfer function [29]. For such a structure, the output noise is extremely low if the proper transfer functions are well controlled. The maximum input range is almost equal to the reference voltage level, and a high SNR for a given oversampling ratio can be achieved. However, the stability and the performance are very sensitive to the nonidealities of the first stage and mismatches, which can result in a serious deterioration of the noise performance of the converter.

The differences in the design challenges of ADC's are reflected by the performance of the state-of-the-art designs found in the literature [29-33]. The performance deficiency seen in ADC's is a result of the nature of the input they process.

For the continuous nature of the analog signals they digitize, ADC's suffer from several problems such as signal and clock skew, clock jitter, nonlinear input impedance, number of components, chip size, and power dissipation. The severity of these problems is somewhat related to the ADC architecture, and sometimes limits the practicality of certain architectures.

In conclusion, as a result of the revolution of digital CMOS design, it is clear that CMOS technology is the dominant process technology in today's semiconductor industry. Further, except for the ultra-low-noise front-end circuit, the most critical circuit in our signal processing loop is the ADC. Thus, this research will investigate ways to develop a high-resolution ADC with a large dynamic range in a CMOS process.

The objectives of this research are:

1) To develop an ultra-low-noise, CMOS digital interface with a large dynamic range for an inertial and tactical grade, single-axis capacitive accelerometer. The optimized micro-gravity, single-axis capacitive accelerometer operates in air and is designed for non-peaking response with a 500 Hz bandwidth.
2) To examine $\Sigma\Delta$ modulator analog-to-digital converter (ADC) topologies from both architectural and circuit level approaches to achieve a large dynamic range at near-DC frequency range.
3) To identify both system and circuit level approaches to implement a $\Sigma\Delta$ modulator demonstrating the techniques developed in this work.

1.3 Organization

This dissertation is organized into four chapters. Chapter 1 introduces the history and development of MEMS accelerometer system, and the motivation behind the work.

In Chapter 2, first it presents the design and the specification of the mechanical sense-element --- a micro-gravity MEMS capacitive accelerometer. Next, a low-noise high-performance switched-capacitor voltage read-out circuit for the micro-g SOI accelerometer is described. The mechanical and electrical elements are analyzed for a clear understanding of factors that affects sensor system noise and sensitivity. Chopper stabilization is selected as a method for removal of offset and flicker noise generated from the electronics. The completely differential electronics enable use of switched capacitor design techniques, relaxing requirements in the CMOS circuit technology. Custom lateral BJT at the input of the op amp is introduced to further reduce the flicker noise of the op amp. Static and dynamic characteristics of the micro-g SOI accelerometer interface are obtained in both 0.6 μm and 0.18 μm process technologies.

Chapter 3 introduces the development of high-performance sigma-delta oversampling ADC, as well as operation and theory. System level simulation and design in Matlab are presented. A complete circuit level design, implementation, and layout consideration are reported. Also the test set-up and characterization of the ADC are presented. Finally, the complete circuit system with read-out front-end circuit and ADC back-end circuit is interfaced to a mechanical MEMS accelerometer and the experimental results is shown at the end of the chapter.

In Chapter 4, the major achievements of this work are summarized and future directions for investigation are outlined.

CHAPTER 2

LOW NOISE SENSING INTERFACE

2.1 Introduction

The readout of the extremely small signal at the output of the mechanical elements is a major challenge in inertial-grade accelerometer design. Typically displacements at a sub-atomic level have to be detected in the presence of large parasitic capacitances at the electro-mechanical interface system. The noise performance of the system will decide the minimum detectable acceleration range; therefore it is a primary concern. In the simplest case of an interface, consisting only of an analog front-end circuit, the resolution is determined primarily by the noise of the switched-capacitor amplifier (capacitive-to-voltage converter), which is the first stage in the signal path, and will be discussed in this chapter. The $\Sigma\Delta$ modulation, which will be presented in the next chapter, on the other hand, introduces quantization errors as additional noise sources.

This chapter is organized as follows. Section I the MEMS capacitive lateral micro-gravity silicon-on-insulator (SOI) accelerometer is briefly presented. Section II introduces op amp design and implementation, which includes the functional diagram of a custom lateral BJT, with its principle of operation and characterizations. Section III presents the interface architecture, design and implementations characterization of a 3 V switched-capacitor (SC) lateral BJT interface circuit in CMOS. Section IV provides the MEMS-IC measure performance and testing results.

The interface circuit is based on a front-end programmable reference-capacitor-less SC charge amplifier. The accelerometer is fabricated through a dry-release high aspect-ratio reduced-gap process. By incorporating the chopper stabilization noise reduction technique in interface circuit, the dynamic range is improved by 10 dB minimum, which leads to a measured resolution of 6.3 μg/√Hz and a dynamic range of 105 dB at 3 Hz. The bias instability was measured at 24 μg for 10 hours with 3.75 mW power consumption. The system was fabricated in a 3 V 0.6 μm CMOS process from MOSIS. Also implementation in 0.18 μm TSMC process, it provides compatible performance. Both have external clocks. A remarkable improvement in the noise performances can be achieved by replacing MOSFET's with lateral BJT's in the input differential couple of op-amps.

2.2 Design of Single-axis Capacitive Accelerometer Device

Capacitive accelerometers are very attractive for high performance micro-g accelerometers duet to their high sensitivity, good DC response and noise performance, low drift, low temperature sensitivity, low-power dissipation, and simple MEMS structure design. The overall sensitivity of a capacitive accelerometer is proportional to the proof mass size, and capacitive overlap area, and is inversely proportional to the spring constant and air gap [13, 26, 34-35]. Therefore, a large proof mass and narrow air gap for high performance accelerometers are required. The devices are required to be all silicon fabricated on a single-wafer to have low temperature sensitivity and good long term stability.

The designed silicon-on-insulator (SOI) accelerometer is fabricated through a backside dry-release process that eliminates the need for release holes in the proof-mass. An extra part of the silicon handle layer in the back of the proof-mass adds more mass and improves the performance.

The fundamental sense limit is set by the Brownian noise equivalent acceleration (BNEA) of the suspended mass. This acceleration, caused by air molecules' collisions, is expressed as [5]

$$BNEA = \frac{\sqrt{4KTD}}{M} = \sqrt{\frac{4KT\omega_n}{MQ}} \propto \sqrt{\frac{h}{(capacitive\_gap)^3}} \qquad \frac{m/s^2}{\sqrt{Hz}} \qquad (2\text{-}1)$$

In this equation, K is the Boltzmann constant, T is the absolute temperature, ω_n is the natural frequency, and Q is the mechanical quality factor. Increasing the mass (M) and reducing the air-damping improves the mechanical noise floor. However, reducing damping causes higher-Q, which is not desirable in this design. Another limiting factor is the circuit noise equivalent acceleration (CNEA) that depends on the capacitive resolution of the interface circuit (ΔC_{min}) and the capacitive sensitivity (S) of the accelerometer ($S = \Delta C$ / gravity):

$$CNEA = \frac{\Delta C_{\min}}{S} \qquad \frac{m/s^2}{\sqrt{Hz}} \qquad (2\text{-}2)$$

The total noise equivalent acceleration (TNEA) of the accelerometer is expressed as

$$TNEA = \sqrt{BNEA^2 + CNEA^2} \qquad \frac{m/s^2}{\sqrt{Hz}} \qquad (2\text{-}3)$$

The design objective is to minimize the BNEA and CNEA per unit area while maximizing the static sensitivity and satisfying process simplicity and size limitations at the same time. The capacitive gap size is reduced by depositing of polysilicon through low-pressure chemical vapor deposition, which relaxes the trench etching process and allows for higher trench aspect ratio (AR = 15) in the 100 μm thick SOI wafer [5].

The design parameters and simulation results from MATLAB and ANSYS are shown in Table 2.1 and Figure 2.1. The SEM picture of one fabricated device is shown in Figure 2.2. The size of the bonding pad for the accelerometer device is 200 μm×200 μm to minimize the parasitic capacitance. It is assumed that the amplification capacitance C_A = 4 pF for the design.

TABLE 2.1: DESIGN PARAMETERS OF TWO ACCELEROMETER DEVICES.

Accelerometer Device (2 μg – 2 g)	**Small-Size, with Added Proof-Mass, 4 Tethers**	**Large-Size, with Added Proof-Mass, 4 Tethers**
Physical Dimensions (μm × μm × μm)	Proof-mass: 2000 × 5256 × 100 Added proof-mass: 1000 × 4256 × 400	Proof-mass: 2000 × 7320 × 100 Added proof-mass: 1800 × 6300 × 400
Capacitive Gap (μm)	2	2
Shock Stop (μm)	1.5	1.5
Tether's Width (μm)	25	40
Tether's Length (μm)	1100	1200
Sensing Electrode's Width (μm)	30	30
Sensing Electrode's Length (μm)	980	980
Number of the Sensing Electrodes	5 × 5 × 4	7 × 5 × 4
Q	0.413	0.77
BNEA (μg/√Hz)	0.777	0.437
CNEA (μg/√Hz)	1.18	1.29
TNEA (μg/√Hz)	1.42	1.36
Maximum g	2 g	2.2 g
Mass (μg)	7.15	13.94
Natural Frequency (Hz)	1646	2033
Pull-in Voltage	4.6	6.9
Air Damping (Ns/m)	0.18	0.25
In-plane Stiffness (N/m)	764	2438

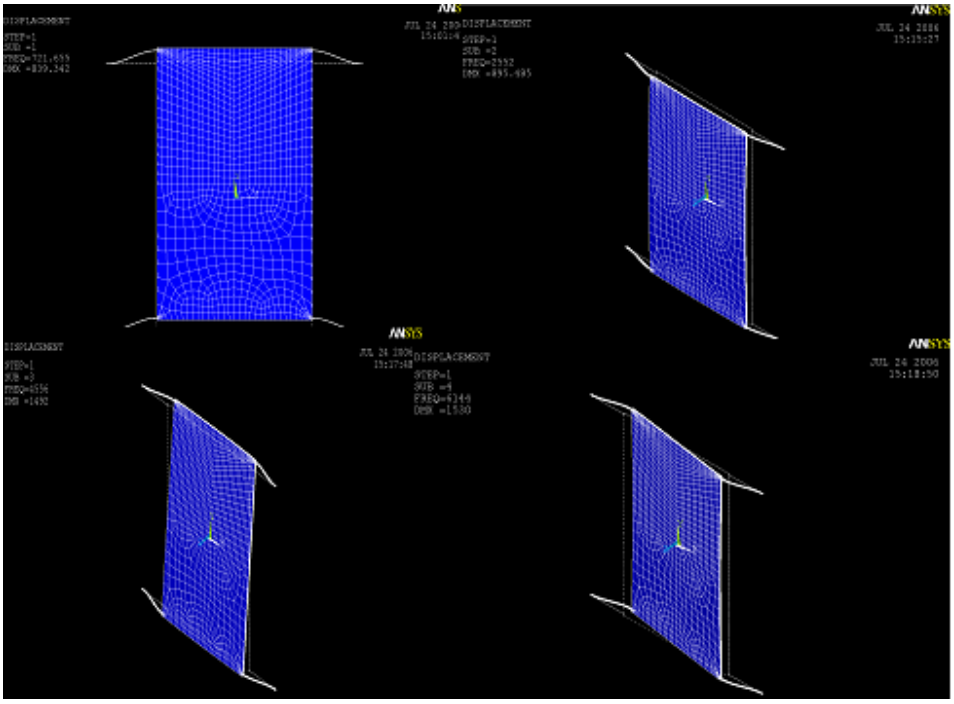


Figure 2.1: Four flexural modes from one prototype device by ANSYS simulation.

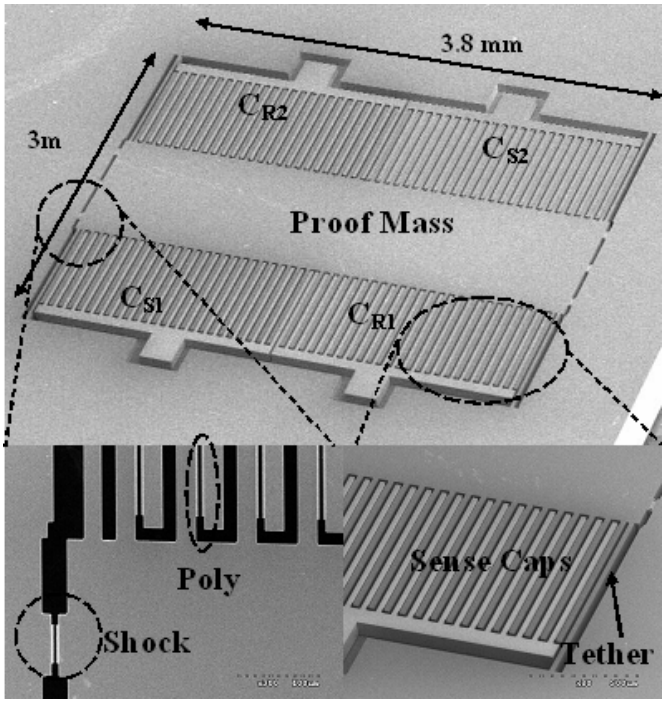


Figure 2.2: SEM picture of the accelerometer fabricated.

2.3 Low Noise Interface Circuit

A micro-g accelerometer should preserve high resolution and stability even at the presence of large DC accelerations such as earth gravity. In open-loop systems, the resolution of the capacitive micro-g accelerometers interfaced with low-cost CMOS is typically limited by the flicker noise of the input transistors from the interface circuit at very low frequencies. Therefore, noise reduction for the accelerometer system is essential to improve bandwidth, dynamic range and linearity.

Although there have been a few reports of micro-g resolution at input frequencies higher than 10Hz, achieving near-DC micro-g resolution has proven to be difficult with small size micromechanical sensors suitable for consumer applications. The correlated-double-sampling (CDS) and chopper stabilization techniques have been successfully implemented to further reduce flicker noise and offsets [2, 7, 13, 28, 36].

In this section, a lateral PNP BJT (LBJT) input interface circuit for a SOI capacitive accelerometer, with a measured resolution of 6 μg/√Hz and the output noise floor of -118 dBV/√Hz at 3 Hz from 0.6 μm AMI process implementation, is presented. Also the implementation in the 0.18 μm TSMC process has show the identical performance. The resolution is further improved by reducing the low-frequency 1/f noise and offset of the LPNP input interface using chopper stabilization technique.

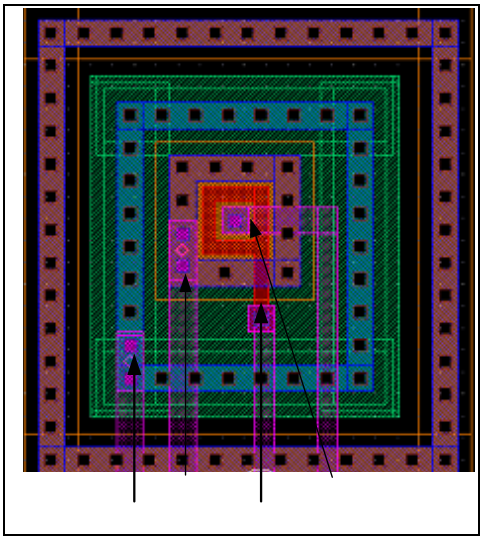
2.3.1 Lateral PNP BJT in CMOS Process

It is widely recognized that lateral BJT's are inherently available in standard CMOS technology [37-38]. Compared with vertical BJT's, these naturally available

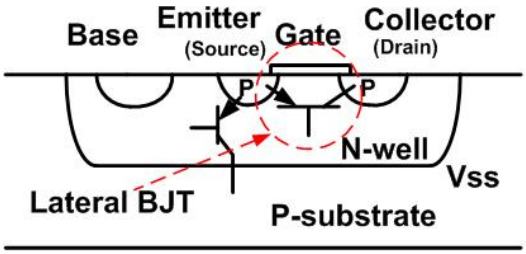
lateral BJT's are suitable for high-performance and low-noise analog circuit applications [39]. Their good matching, high transconductance and very low 1/f noise make them attractive for use in amplifiers. They are fully compatible with conventional, low cost CMOS process.

Lateral NPN BJT had been extensively used in a 6μm p-well CMOS technology and applied these devices to dc circuits such as voltage references and operational amplifiers [40]. To access the feasibility of using the lateral PNP BJT, we report here the results of extensive measurements on bipolar test structures fabricated in a production of 0.6μm n-well CMOS AMI process provided by MOSIS and 0.18μm CMOS TSMC process. Because the characteristics of the lateral BJT's are determined by the dimensions, doping level in the well and substrate, they might not scale in the same way as MOSFET's in a short-channel CMOS process.

Figure 2.3 illustrates the lateral PNP (LPNP) bipolar transistor in a CMOS p-channel device at 0.6μm AMI CMOS process. The source, drain, and n-well of the p-MOSFET serve as the emitter, collector, and base of the LPNP device, respectively. The performance of the lateral device greatly depends on its layout. The emitter area and lateral base width (the channel length L of the corresponding MOSFET) should be minimized, and the emitter should be completely surrounded by the collector.



(a)



(b)

Figure 2.3: (a) the custom layout at 0.6 μm process and (b) Lateral PNP BJT diagram.

To improve the lateral collector current efficiency and noise characteristics, the LPNP transistors are laid out as multi-emitter devices, where each emitter dot is a minimum area p-diffusion contact surrounded by a polysilicon gate. To prevent the latch-up problem each device is surrounded by a p+ substrate guard ring. For proper operation, the gate must be zero-biased with respect to the emitter to prevent the PFET transistor between the collector (drain) and emitter (source) from turning on. A small positive bias on the gate is preferred, with a gate-emitter voltage of above 200 mV or more providing

good results. Most importantly, this positive biasing of the gate drives the diffusion minority carriers in the base (under the gate oxide) deeper into the n-well and away from the surface defects, thereby reducing 1/f noise at low frequencies [40-41]. Although the lateral BJT offers a free collector, making it desirable for use in a circuit, it only collects a fraction α of the emitter current; the remaining fraction is collected by the vertical BJT that is always biased in the forward active region. This α is determined by the sidewall-to-area ratio of the emitter diffusion [37-38].

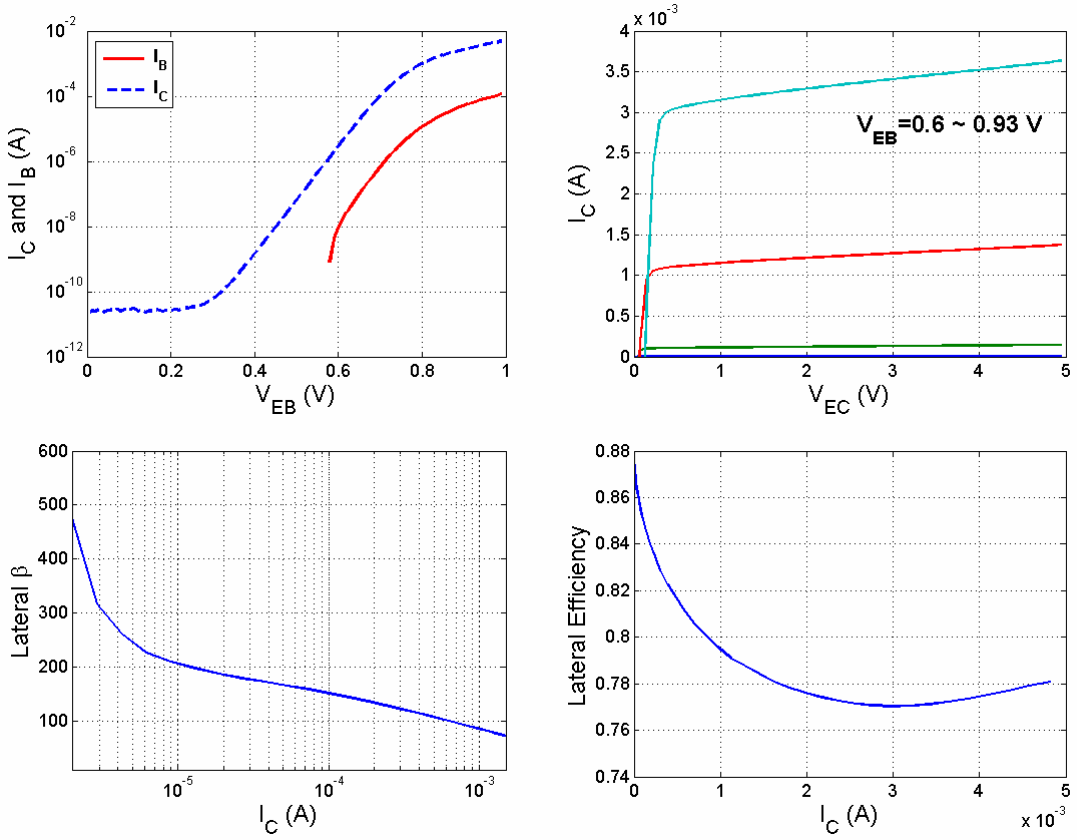


Figure 2.4: Main dc characteristics of 40-emitter-in-parallel LBJT from 0.6 μm process.

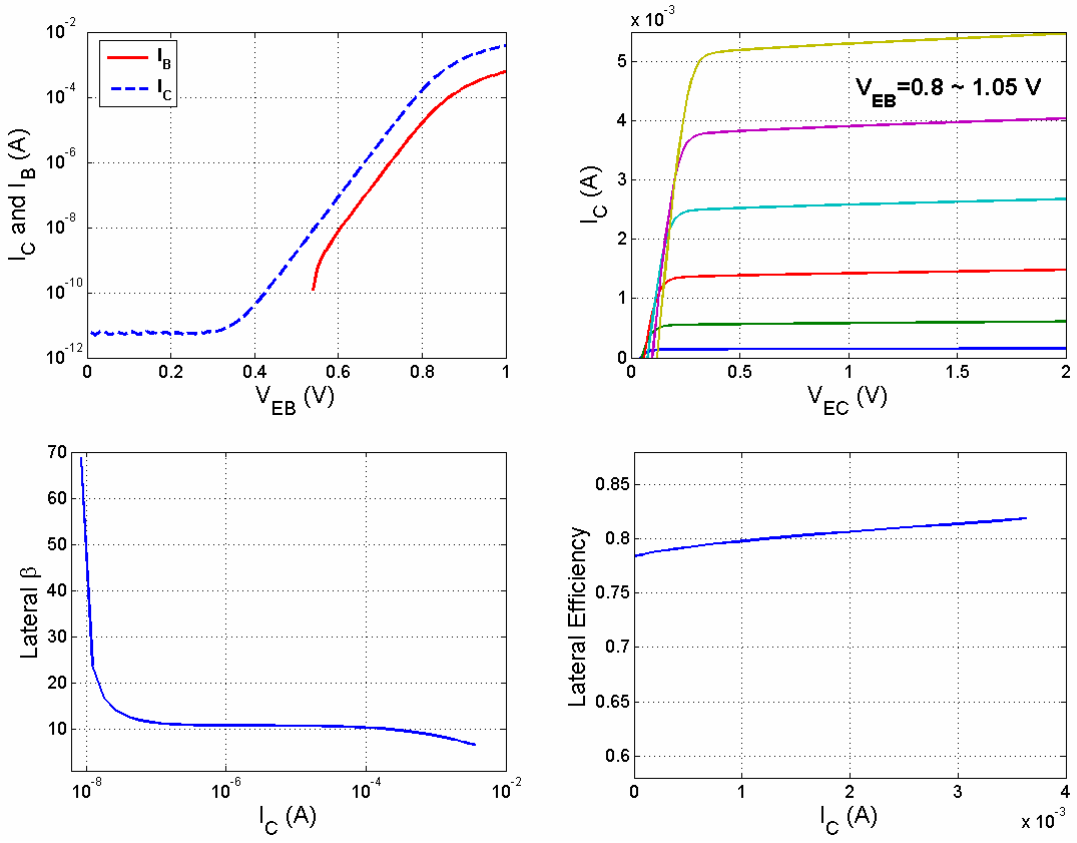


Figure 2.5: Main dc characteristics of 40-emitter-in-parallel LBJT in 0.18 μm process.

On-wafer *dc* and *ac* test structures were fabricated in two separate runs; measurements were made to characterize the device performance at room temperature. An Agilent 4155 parameter analyzer and an Agilent E8364B network analyzer were used for the measurements.

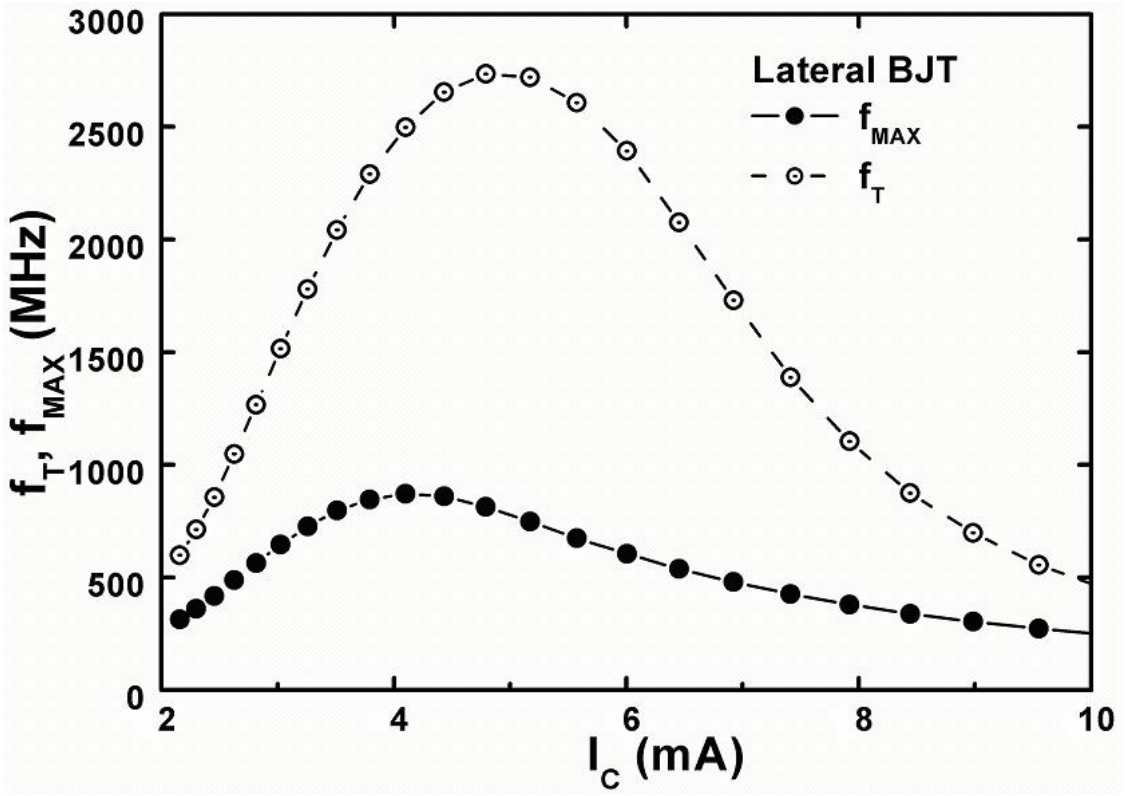


Figure 2.6: The measured cut-off frequency (f_T) and the maximum oscillation frequency (f_{max}) as functions of collector current (I_C) for a LBJT from 0.18 μm TSMC process.

All measured devices have emitter areas of 0.6×0.6×40 (40 emitters in parallel configuration) μm^2 in the 0.6 μm AMI process. Figure 2.4 shows the Gummel characteristics indicating the feasibility of these devices for real circuit applications. The main dc parameters for this 40-emitter-in-parallel LPNP BJT from 0.6μm process were measured as follows: lateral β = 150 at 10 μA collector biasing current, which is the same biasing for the input branch of the OTA. Within this operating range, the lateral efficiency of the transistor ranges from 0.77 and 0.87, with lateral efficiency defined as

$$Efficiency_{lateral} = \frac{I_{C\_lateral} + I_B}{I_E} = \frac{I_E - I_{C\_vertical}}{I_E} \quad (2\text{-}4)$$

where $I_{C\_lateral}$ and $I_{C\_vertical}$ are the lateral and vertical collector current, respectively. The lateral efficiency measured is 0.86 at 10 μA, and the extracted Early voltage is 28 V. The 1/f corner frequency was less than 1 KHz. As expected, the lateral PNP BJT transistor had much improved low frequency noise performance compared to a standard PFET.

Figure 2.5 shows the main dc parameters for LPNP BJT fabricated from 0.18μm TSMC process. The lateral β is 12 at 10 μA collector biasing current. The different doping profiles in the AMI and TSMC manufacturing processes contributed the β variation in the measurements [42].The lateral efficiency achieved is 0.8, and the extracted Early voltage is 29 V. The measured f_T and f_{max} *vs*. collector current (I_C) for the 40-emitter-in-parallel LPNP BJT at room temperature are plotted in Figure 2.6. The f_T and f_{max} values were extracted from h_{21} and Mason's U that were converted from the measured S-parameters. Both h_{21} and U at each bias point show -20dB/dec roll-off at the extrapolating frequency. The peak f_T reaches 2.73 GHz. The high parasitics related to the lateral bipolar structure results in lower f_{max} that peaks at 870 MHz. However, the device speed is more than adequate for the proposed application.

2.3.2 The OTA Design

The transistor-level simulation of the designed interface circuit is performed using Cadence, and time-varying capacitances (representing the accelerometer's changing sense capacitances) are modeled in Verilog-A. The chip manufacturings are implemented

both in the 3 V 0.6 μm AMI CMOS process from MOSIS and the 0.18 μm TSMC process. All the accelerometers and the IC layouts are drawn in Cadence Virtuoso. A complete design and evaluation cycle, including parasitic capacitance extraction, layout-versus-schematic (LVS) comparison, and post-layout simulation, are carried out before each IC submission.

For a typical CMOS amplifier used in the interface circuit to an accelerometer, the equivalent input referred noise voltage is usually dominated by the MOS input transistors of the differential input stage. Because 1/f noise in a MOSFET is inversely proportional to the square root of the gate area, the 1/f noise of a MOSFET in CMOS amplifier can be reduced to some extent by increasing its gate area. Such type of low-noise amplifier has been constructed using this technique, but with the inevitable penalties of greatly increased area requirements and large input capacitances [43-44].

Another alternative to large geometry MOS transistors is a BiCMOS process where bipolar transistors are used at the input stage. Bipolar transistors have much less 1/f noise with 1/f noise corner frequencies typically around 100 Hz and lower [45]. However, the process complexity of the BiCMOS results in higher costs. Compared to conventional vertical PNP devices that exhibit very impressive low noise performance, the optimized lateral PNP BJTs, which is available in standard CMOS process, exhibit comparable low-frequency noise performance to their vertical counterparts and better than the standard PMOS transistors [39, 40, 46].

The special characteristics of the switched-capacitor circuit impose dramatic limitations on the OTA core in the interface circuit design. For high-sensitivity capacitive

SOI accelerometers, the sensing capacitor is very large, so the rest capacitance is also large, which imposes limitations on the performance of the OTA and the interface circuit. The fully differential SC-circuit structure is chosen for its higher PSRR, lower harmonic distortion, lower the noise. It also means larger op-amp and more power.

Folded-cascode architecture with a standard gain-boosting technique is chosen for the fully-differential OTA in the switched capacitor voltage amplifier [40]. It further increases the output impedance without adding more cascode transistor stages. It is a low-power low-noise fully-differential OTA with a very high DC gain that improves the functionality and noise performance of the switched-capacitor circuit. Table 2.2 shows the design specifications of the OTA that will be used for the core in the front-end and back-end circuits.

The transistor level schematic of the implemented OTA is shown in Figure 2.7. And its simulated frequency response is shown in Figure 2.8. The OTA is self-compensated via the loading capacitances. The input stage of the OTA utilizes lateral PNP BJT's (M1, M2) to reduce the flicker noise and its corner frequency. The transconductance of the input transistors is large enough to minimize the noise contribution from other transistors when the noise is reflected to the input. The optimized dimensions for the LPNP BJTs as the input stage are devised and characterized in both CMOS processes. Four error amplifiers (A1 and A2) are used to increase the output impedance. They keep the active load pairs (M3, M4, M9, and M10) to operate close to the edge of the ohmic region with the equal drain-source voltages that maximize the output differential swing and maintain their constant biasing currents. The bias voltages V_{B1}, V_{B2} are generated from a bootstrapped voltage reference biasing circuit. A

continuous time differential averaging amplifier (DAA) configuration is used for the output common-mode feedback circuit (CMFB). The OTA can provide a differential output swing of 4 V from a single supply of 3 V.

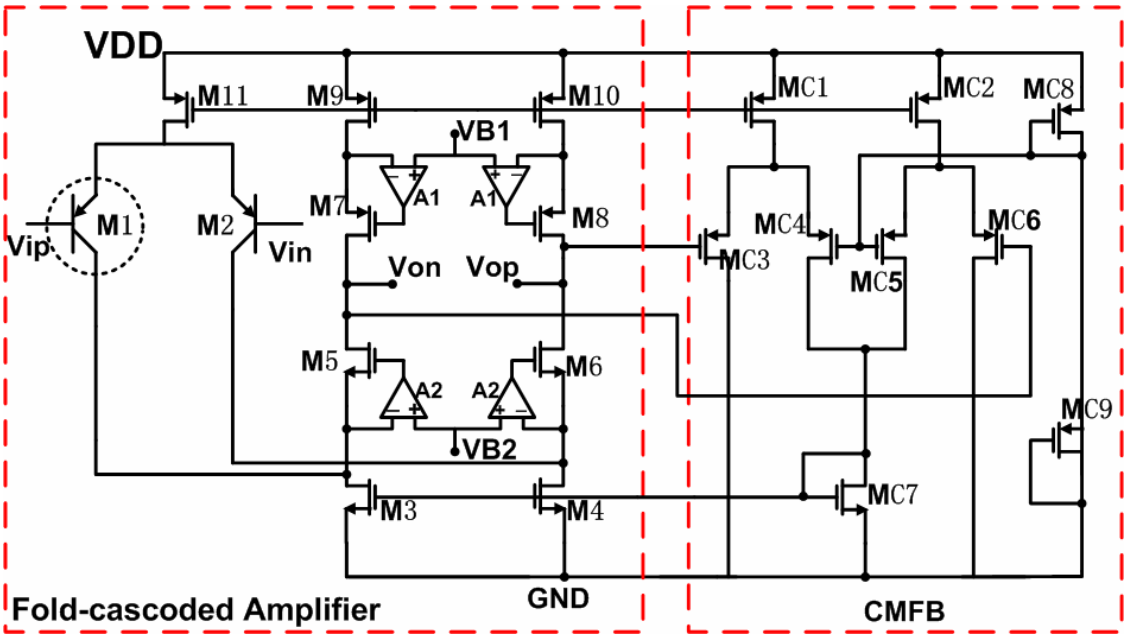


Figure 2.7: Schematic of a gain-boosted folded-cascode OTA with input stage using LBJT.

TABLE 2.2: DESIGN SPECIFICATIONS OF A FULLY DIFFERENTIAL OTA

Design Parameters	**Values**
Power Supply	3 V
Differential Output Swing	4 V
Common-mode Output Voltage	1.5 V
Gain	> 100 dB
Unity-gain-bandwidth	> 5 MHz
Phase Margin (PM)	> 60 degrees
Common-mode Rejection Ratio	>80 dB
Total Currents	200 μA

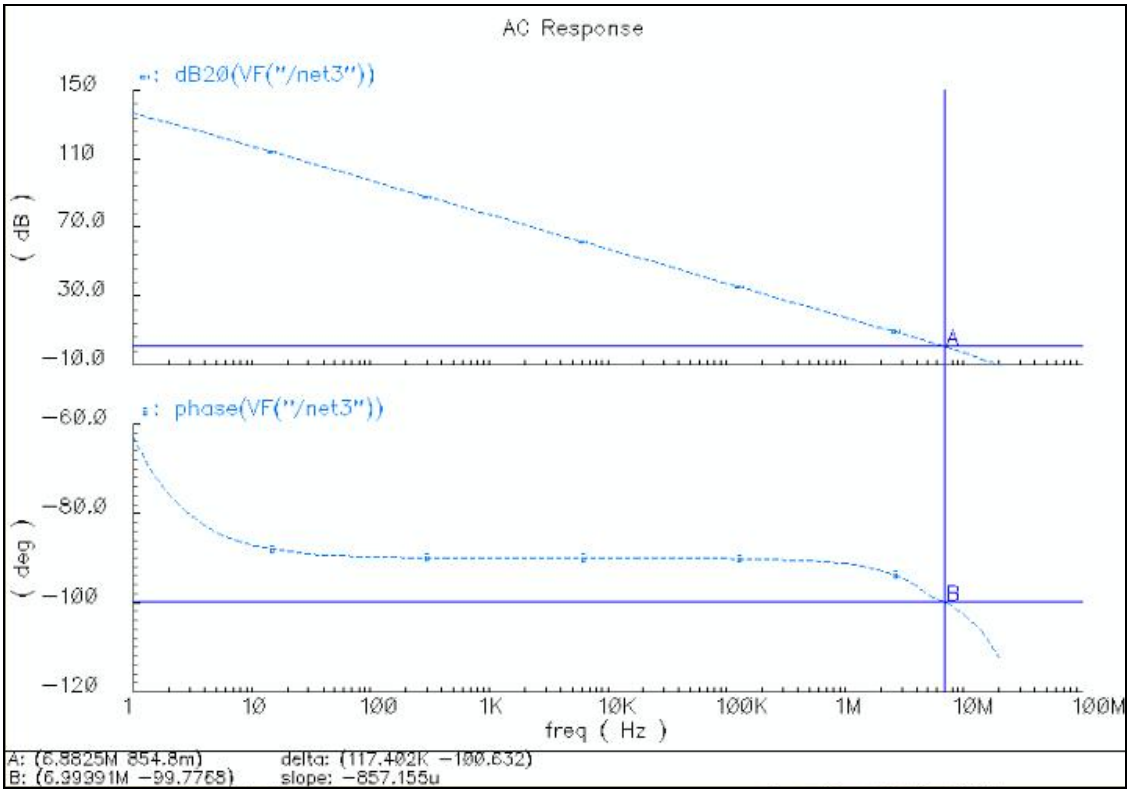


Figure 2.8: The simulated frequency response of the OTA.

2.3.3 Interface Architecture Implementation

In this section, the interface with the chopper-stabilization technique is introduced with the goal of a further noise reduction at the low-frequency range. Moreover, a fully differential scheme is used to reduce the common-mode noise. Gain multiplexers have been set to provide the capability of interfacing accelerometers with different sensitivities.

In the presence of large parasitic capacitances, the extremely small signals at the output of the mechanical elements have to be detected at the electro-mechanical interface system. Both mechanical offset and electrical noise contributed from fabrication errors

affect the overall open-loop/closed-loop accelerometer resolution. High-precision capacitive accelerometers were achieved by reducing the low-frequency noise and offset cancellation techniques.

In previously reported capacitive accelerometer interfaces, on-chip reference capacitors were necessary to form a balanced capacitive bridge and set the input common-mode voltage of the amplifier [7, 13]. Moreover, the proof mass was typically switched between supply (V_{DD}) and ground, which required a digital circuit capable of driving the parasitic capacitance between the proof mass and substrate. In an effort to eliminate area-consuming on-chip reference capacitors, in this architecture, reference capacitors are absorbed in the sense capacitance of the accelerometer without compromising the sensitivity of the device or increasing area [28, 46]. This also helps to further reduce the clock noises and improve the power dissipation. The sense capacitance is split into four identical sub-capacitances in a fully symmetric and differential manner (two increasing and two decreasing). This architecture provides a better versatility in accommodating different capacitive sensors. The differential output voltage (V_O) is given by:

$$V_O = V_{OA1} - V_{OA2} = \frac{\Delta C_S}{C_A} V_{DD} \tag{2-5}$$

where ΔCs is the sensor differential capacitance change due to an input gravity/acceleration, C_A is the amplification capacitor of this voltage amplifier, V_{DD} is the dc power supply.

To reduce the effect of the op-amp offset and low-frequency noises, CDS was proposed in [28, 47, 47]. In that work, a 40 μm thick SOI microaccelerometer with

resolution of sub-100 μg/√Hz and sensitivity of 0.2 pF/g had been presented. In [28, 47], through innovation in MEMS process and interface IC design, the resolution and sensitivity of the dry-released SOI accelerometers are each improved to achieve μg/√Hz level resolution and stability in a small form-factor (<0.4cm^2). The detailed fabrication process of the SOI accelerometers was also presented.

Figure 2.9 shows the overall architecture of the implemented fully-differential microaccelerometer interface IC. Φ_1 and Φ_2 denote inverted sampling clocks, and Φ_{chop1} and Φ_{chop2} denote inverted chopping clocks. This interface IC uses a fully-differential input/output architecture for its harmonic reduction and PSRR improvements. It includes a reference-capacitor-less SC charge amplifier with a programmable gain of 0.5, 1 and 2. In contrast to conventional CMOS interface architectures [2, 7, 13, 28, 36], this architecture introduces the lateral PNP BJT at the input stage to reduce the flicker noise at very low frequencies. In addition, it integrates the chopper stabilization technique [49-51] into the LPNP switched-capacitor voltage amplifier to further reduce flicker noise and DC offset, which is superior to the interface implemented in full CMOS transistors under the same circumstances.

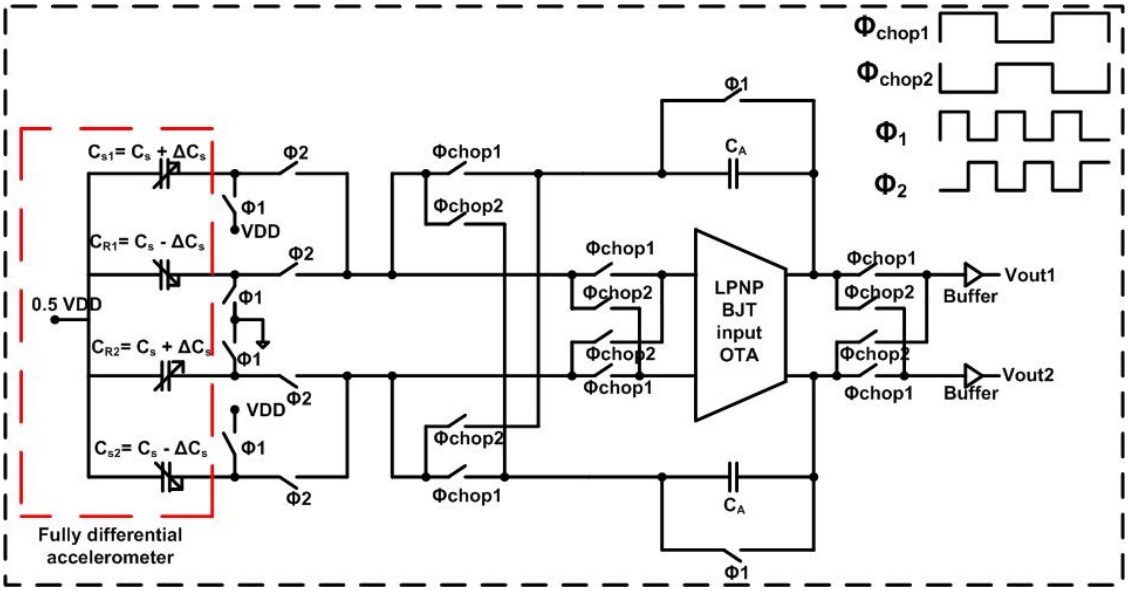


Figure 2.9: Schematic of a switched-capacitor chop-stabilized interface.

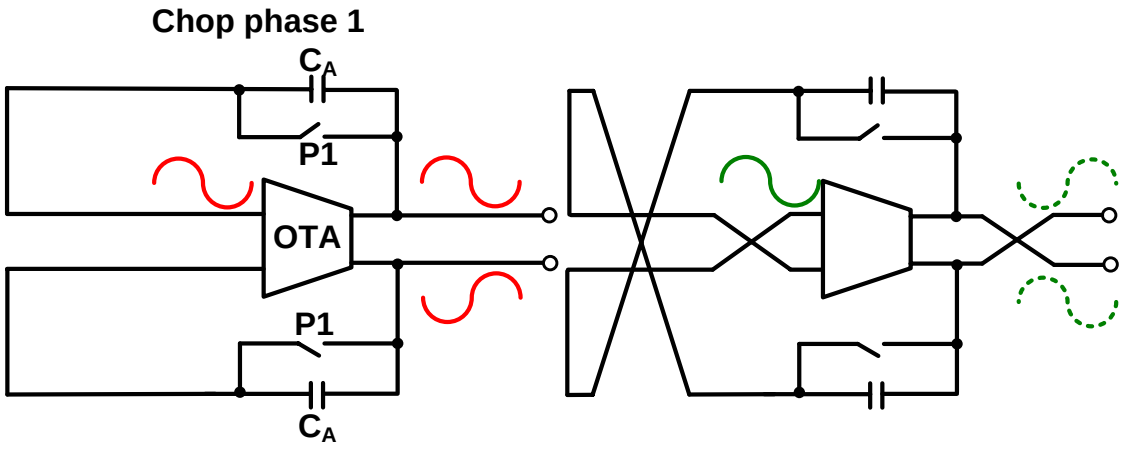


Figure 2.10: Noise reduction scheme of the chopper stabilization technique.

The elementary operation of the chopper stabilization for a differential signal, noise, and offsets has been extensively discussed in [49-51]. Contrary to the CDS technique, the white noise is not aliased because there is no sample-and-holder process. The chopper amplifier is a time-variant system, which is inherently nonlinear. However,

with regard to a bandwidth limitation of the input signal far less than the f_{chop}, the amplifier behaves as a quasi-linear system in the frequency range considered. Since the spectral envelop is inversely proportional to the frequency, the output signal after amplification and demodulation is essentially reconstructed by the fundamental components. This set the problem of choosing the amplifier bandwidth such as to have sufficient gain for the modulated signal while rejecting most of the spikes' spectral components, and also providing proper settling of the amplifier. The band-limitation requirement is usually satisfied in low-frequency sensor applications. And the f_{chop} can be chosen accordingly by taking into account that the residue offset increases proportionally as f_{chop} increases. 1/f noise is completely removed if the chopping frequency is higher than 1/f corner frequency. The offset of the chopper amplifier is limited by charge injection mismatch. The charge injection and parasitic coupling in the input nodes of the OTA cause spikes to appear.

The schemes of the sampling and chopping frequencies were devised to achieve proper operation. A chopping frequency at 1/2 of the sampling frequency has been found to be most effective because it shifts the op-amp imperfections farthest away from the signal band. Both clocks were generated externally. The CMOS complementary switches are used to reduce the clock feedthrough and charge injection of the switches. For one chopping clock period in Figure 2.10, during chop phase 1, the noise at the input of the operational transconductance amplifier (OTA) is amplified at output. During chop phase 2, the noise is crossed over (through different branches) by the chopping scheme and amplified at the output. The noise at the fully differential outputs will be averaged out.

All the switches inside this SC circuit are implemented with transmission gates. The switches require relatively constant on resistance in order to minimize distortion caused by the nonlinear on resistance of switches. Therefore, the aspect ratio of PMOS devices in transmission gates is taken to be 3 times larger than those of NMOS devices in order to maintain relatively constant on resistance.

The purpose of the input biasing is to establish the dc voltage at the input nodes of the OTA and also to prevent unwanted charging activities. The large impedance nodes of the sensor require large impedance at the input of the OTA. In our design, the biasing for the base of LPNP BJT in our IC is provided by the switching mechanism through the sampling and chopping switches in the feedback loop, which is more robust than the traditional biasing methods such as diodes and subthreshold MOSFET's, and does not require any tuning.

The biasing for the base of LPNP BJT in our IC is provided by the switching mechanism through the sampling and chopping switches in the feedback loop. Large β (200) achieved in the 0.6 μm AMI process, has reduced the requirement of the base biasing current to around 80 nA. For one sampling clock period, during the reset phase (P1 is closed), the inputs of the OTA are connected directly to the dc voltages at the outputs of the OTA through the switches in the feedback loop. During the amplification stage, the amplification capacitance C_A's and the rest sampling/chopping switches in the feedback loop around the OTA, which behave as large resistors, provide the proper base currents of the OTA. This fast periodic switching scheme on the feedback loop around the OTA is also called as dynamic biasing in different names, which not only improves

the low-frequency noise performance, but it also provides the dynamic biasing for these lateral BJT inputs of the OTA, thus the mismatches of β of BJT's are minimized.

Low-frequency noise reduction is an important requirement in accelerometer interfacing, which improves the resolution of the system. The resolution at the output is limited by the noise sensitivity of the interface circuit given by

$$Resolution \propto \frac{C_A \cdot V_{noise}}{V_{DD}} \tag{2-6}$$

In order to compare the effectiveness of different noise reduction techniques while they are interfaced with the same accelerometer device, the interface circuits implemented with CDS, chopper stabilization with lateral BJT at input stage, and chopper stabilization with standard PMOS at input stage, are designed and fabricated together in the 0.18 μm TSMC process. The OTA's used in those designs have the identical core design specifications, which are described previously.

The CMOS chopper amplifier as the interface circuit using chopper stabilization with standard PMOS at input stage of the OTA is designed in the 0.18 μm TSMC process, which shares the identical architecture and operation principle as shown in Figure 2.7.

The CMOS CDS amplifier designed as the interface circuit using CDS noise reduction technique is based on the prototype circuit developed in [28, 47]. As shown in Figure 2.11, at the sampling phase (Φ1=high), the two CDS capacitors C_{CDS} accumulate and save the offset and instant low-frequency noises. At the amplification phase (Φ2=high), the accumulated charge in C_S and C_R transfers to C_A, and C_{CDS} cancels out the slowly-changing offset and instant low-frequency noise. Using the charge

redistribution and conservation from the sampling and amplification phase, the differential output voltage is proportional to the ratio of the sense capacitance change (ΔC_S) and amplification capacitance C_A, same as shown in (2-5).

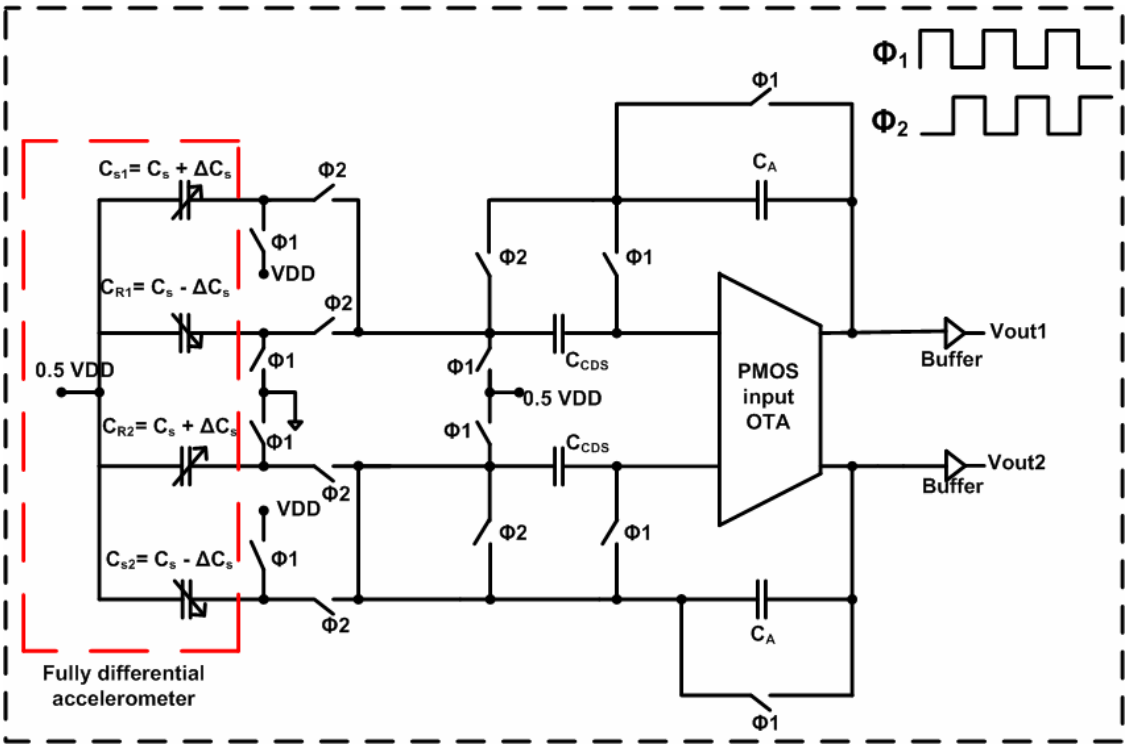


Figure 2.11: Schematic of a switched-capacitor interface circuit using CDS techniques.

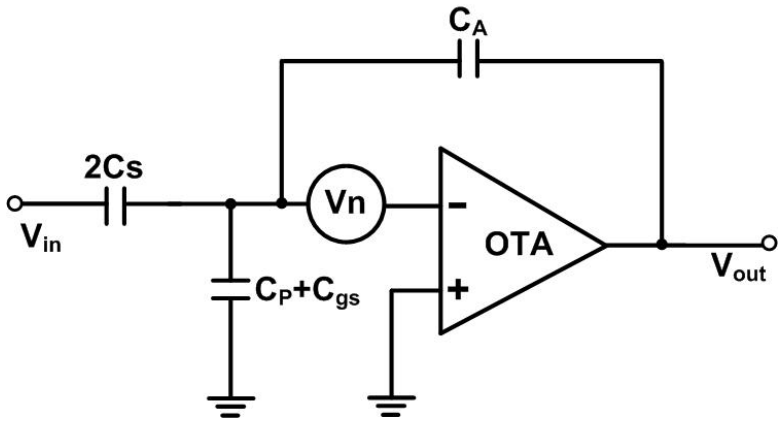


Figure 2.12: Noise representation for op-amp input-referred noise analysis.

The input referred noise for one accelerometer interface circuit is mainly dominated by the flicker noise of the op-amp, and the white thermal noise. For clear analysis, the op-amp noise analysis in a single-ended representation of the differential topology is shown in Figure 2.12 and 2.13. Application of chopper stabilization technique effectively reduces the effects of the flicker nose, thus can be ignored here. The voltage fluctuations at the op-amp input cause changes to flow onto the amplification capacitance from both the sense and the parasitic capacitors, causing the op-amp noise to be amplifier by a factor of

$$V_{out} = \left(\frac{C_A + C_p + C_{gs} + 2C_S}{C_A} \right) \times V_n \tag{2-7}$$

where C_p is parasitic capacitance, $2C_s$ are the two rest capacitors connected to the input nodes of the op-amp, C_A is the amplification capacitance. The power spectral densities of the input-referred-noises of all three implementations with lateral BJT chopping, CMOS chopping and CMOS CDS techniques, which are all fabricated in the 0.18 μm TSMC process, are shown in next part.

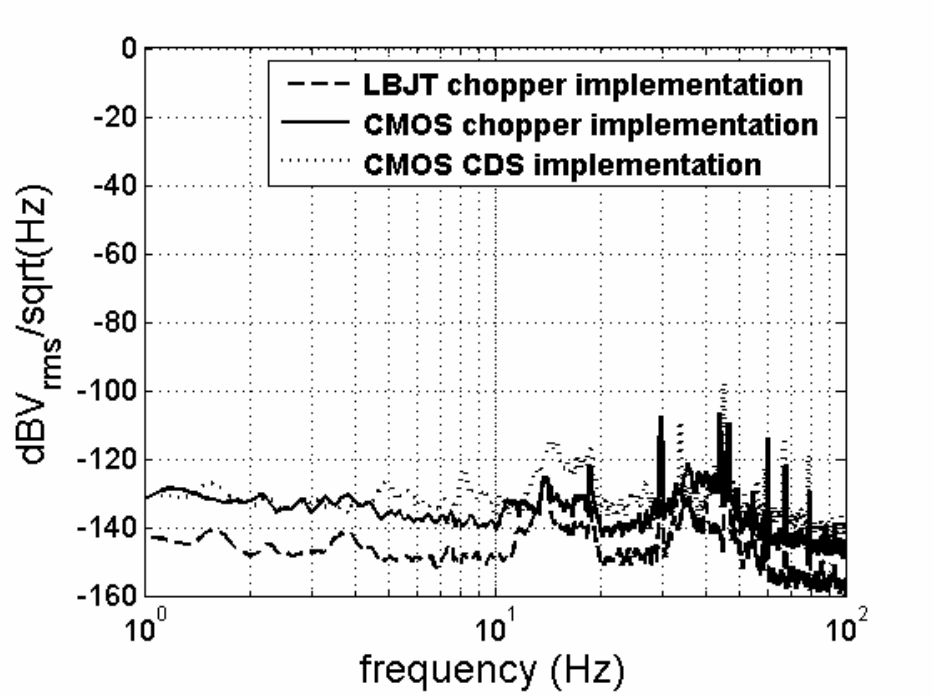


Figure 2.13: A comparison of the input-referred noise for implementations with LBJT chopping, CMOS chopping and CMOS CDS techniques in 0.18 μm TSMC process.

2.4 Interface Measurement Results

Fabricated SOI accelerometers are wire-bonded to the IC chips fabricated in both processes and are tested for its static and dynamic responses.

For the interface circuits fabricated from 0.6 μ m AMI process, the time response is shown in Figure 2-14. As in Figure 2.15, the chopping scheme reduces the flicker noise at the outputs of the interface to -118 dBV/ √ Hz at very low frequencies. The sampling frequency is 600 KHz while the chopping frequency at 300 KHz. The results are compared with implementations that do not utilize chopping scheme, and with regular PMOS-input implementation that uses the same OTA with CDS at different gains. As

partly shown in [46], the interface system provides a noise reduction of 15 dB, corresponding to a dynamic range of 105 dB at 3 Hz bandwidth. The CMOS-SOI accelerometer is tested for the bias instability over 10 hours in a laboratory environment to be 23.79 μg. The bias instability is extracted using the Allan Variance analysis, as shown in Figure 2.16.

The chopper-stabilized lateral-BJT-input interface in CMOS achieves the lowest noise floor at low-frequency range. It provides a minimum 10 dB noise reduction as shown in Figure 2.15 and 2.16. Based on the measurements from the IC's made both 0.6 μm and 0.18 μm processes, as long as the base biasing requirement for the lateral BJT's of op-amp is small, even with β variation, it's suitable to integrate them into standard CMOS circuits to achieve extremely low-noise performance at low frequencies. For the TSMC process implementation, the bias instability was tested to be 22.9 μg with a sensitivity of 135 mV/g at the chopping frequency of 100 KHz as shown in Figure 2.18. The micrographs of the IC dies fabricated in AMI and TSMC processes, respectively are shown in Figure 2.19. The micrograph of the prototype testing chip fabricated in 0.6 μm AMI process on the left in Figure 2.19. The die picture of an SC voltage amplifier at the 0.18 μm TSMC process is on the right. The active area of the chip, which includes OTA and switched-capacitor circuit, occupies 1.96 mm^2 for AMI process, and 1 mm^2 for TSMC process, respectively.

Table 2-3 shows the summary of the measured specifications of the sensor and the interface IC chip made from both 0.6 μm AMI process and 0.18 μm TSMC process. Part of the results measured from IC fabricated from the 0.6 μm AMI process were presented in [46]. The accelerometer requiring 2 μg to 2 g range, which the SEM is shown in Figure

2.2, is fabricated on a SOI wafer using a unique process similar to the one described in [28].

TABLE 2.3: SUMMARY OF RESULTS

Sensor Specification		
Device Size	3.8 mm x 3 mm x 0.5 mm	
Rest Capacitance	10 pF	
Sensitivity	0.1 pF/g	
Brownian Noise Floor	1 μg/√Hz	
IC Specifications		
Chopping Frequency	300 kHz, with 600 kHz sampling frequency for main circuit	100 kHz
Dynamic Range	105 dB @ 3Hz, with 1Hz RBW	106 dB @3Hz, with 1Hz RBW
Sensitivity	204 mV/g	135 mV/g
Minimum Detectable Acceleration	15.8 μg @ 1Hz (RBW=1Hz) 6.29 μg @ 3Hz (RBW=1Hz)	9.35 μg @ 1Hz (RBW=1Hz) 5.88 μg @ 3Hz (RBW=1Hz)
Capacitance Resolution	1.054 aF @ 1Hz (RBW=1Hz) 0.42 aF @ 3Hz (RBW=1Hz)	0.42 aF @ 1Hz (RBW=1Hz) 0.265 aF @ 3Hz (RBW=1Hz)
Power Dissipation	3.75 mW (± 1.5 V)	4.5 mW (± 1.5 V)
IC Die Size	1.96 mm^2 (0.6 μm process)	0.05 mm^2 (0.18 μm process)

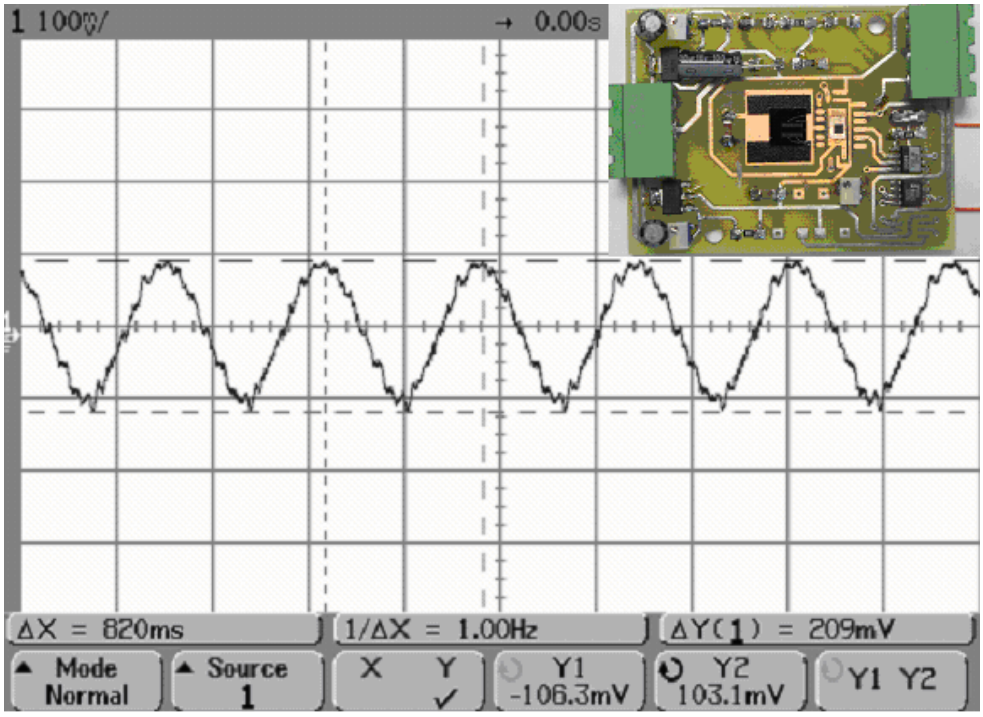


Figure 2.14: Accelerometer output response to 1Hz, ±0.5 g acceleration (0.6 µm AMI).

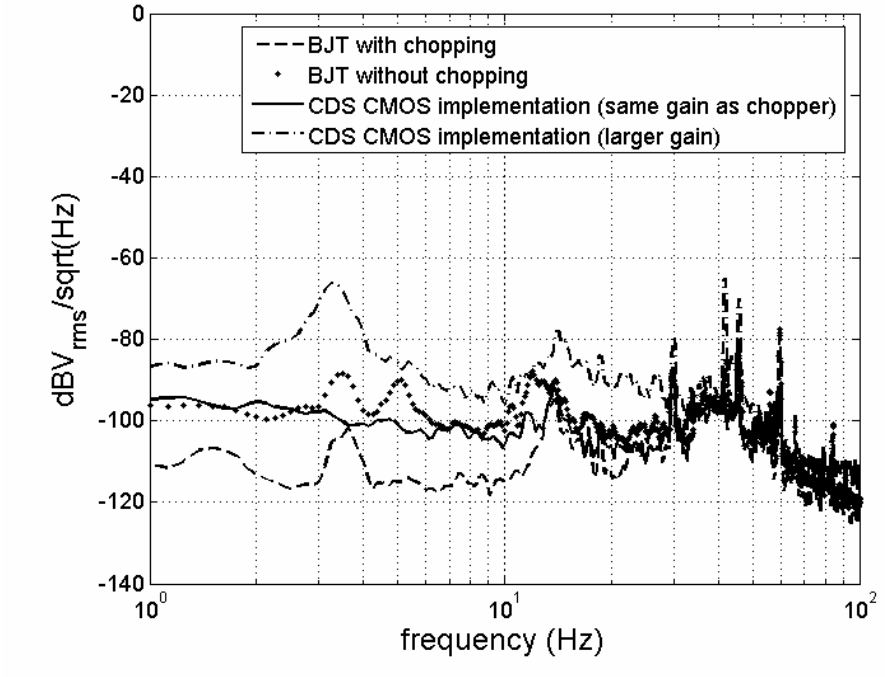


Figure 2.15: Measured output noise of interface system (0.6 µmAMI).

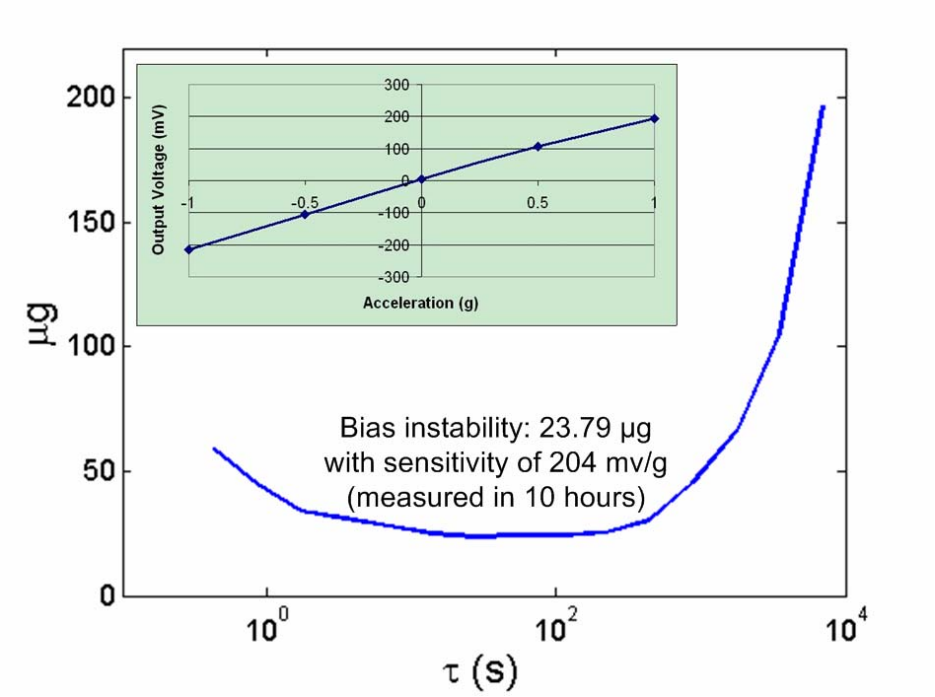


Figure 2.16: Allan variance plot of the overall system (0.6 μm AMI) output showing an in-run bias instability of ~24 μg at room temperature.

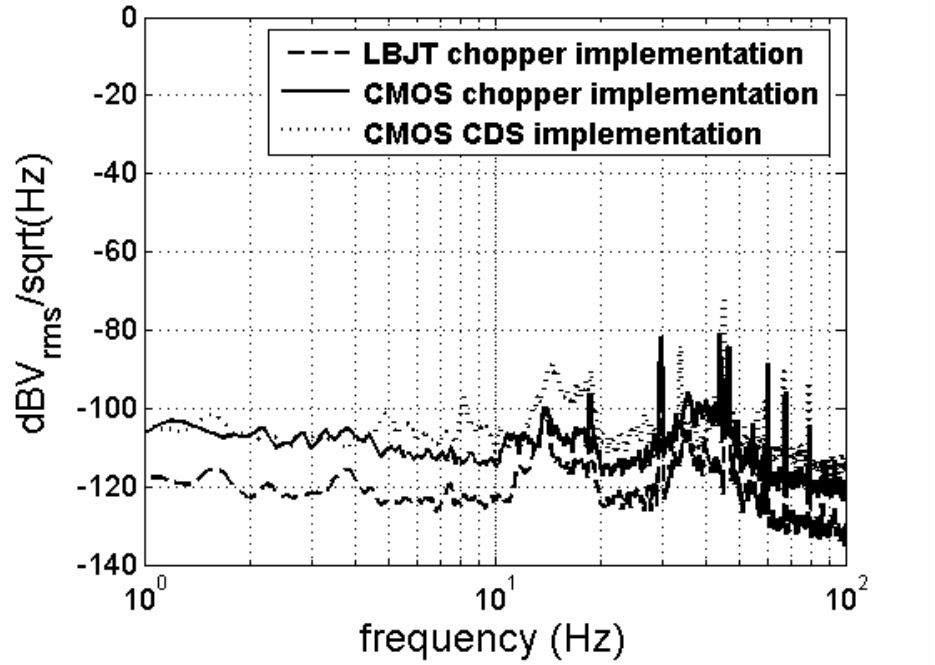


Figure 2.17: Measured output noise of interface system (0.18 μm TSMC).

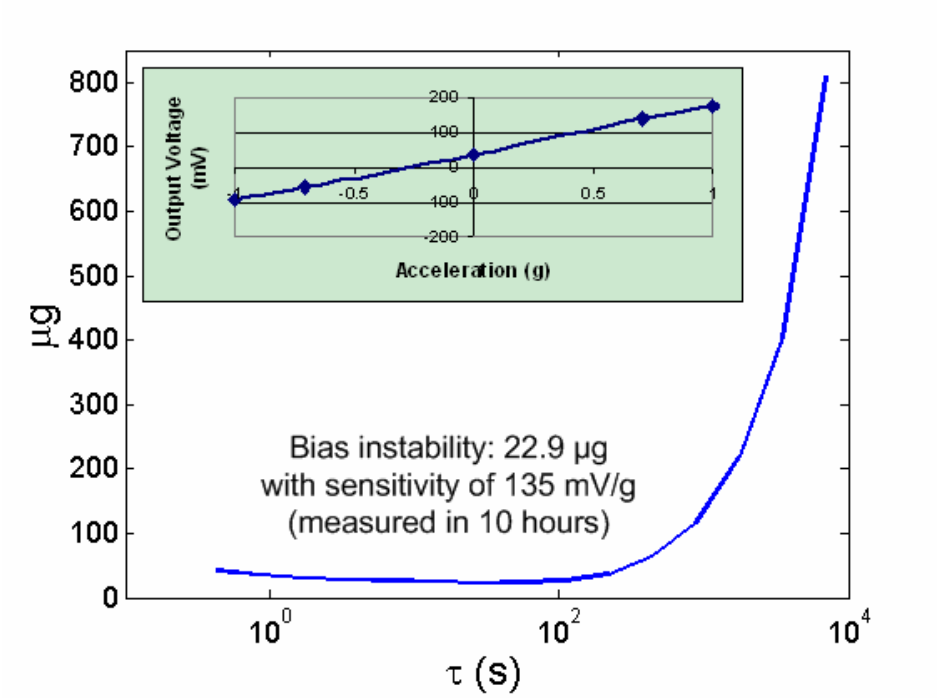


Figure 2.18: Allan variance plot of the overall system (0.18 µm TSMC) output showing an in-run bias instability of ~23 µg.

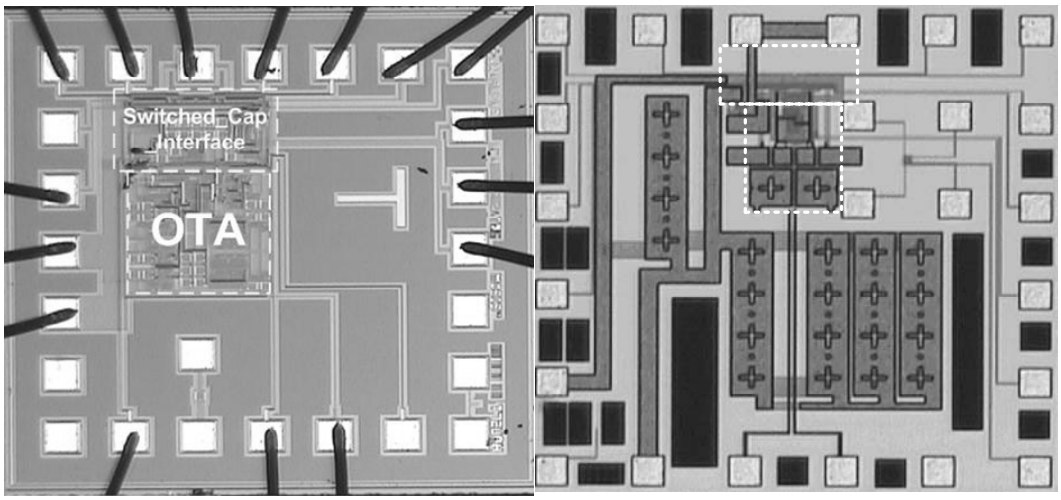


Figure 2.19: The micrographs of the IC dies fabricated in AMI (left) and TSMC (right) processes.

2.5 Conclusion

The implementation and characterization of chopper-stabilized lateral-BJT-input interfaces in CMOS for capacitive accelerometers with micro-gravity resolution and stability are presented. Their good matching, high transconductance and very low 1/f noise make them attractive for use in amplifiers. The full compatibility with conventional, low cost CMOS process suggests competition with BiCMOS approaches for mixed analog/digital applications. A reference-capacitor-less front-end IC is implemented with the ability of interfacing different capacitive accelerometers, which application can be extended to capacitive pressure sensors [52] as well. The effectiveness of low-frequency noise reduction through chopper stabilization in comparison with CDS scheme had been measured by comparing the noise spectrum of the interface systems. A minimum10 dB improvement in noise reduction and hence 105 dB dynamic range are achieved at low frequency near DC range [46].

CHAPTER 3

SIGMA-DELTA ADC

3.1 Introduction

Sigma-delta converter was first introduced in 1962 [53], and is the most widely used oversampling converter, simply because it is the most robust ADC against circuit imperfections.

Sigma-delta modulators have applications in the telecommunications and audio industries as a means of A to D conversion, especially for high accuracy. High order modulators are employed to obtain an improved signal to noise ratio. However, due to this high order, such system may be become conditionally stable and may exhibited complex in the phase space, hence such devices are more difficult to stabilize and implement in hardware. Consequently, they are suited for slow and medium speed conversions such as instrumentation, digital voice, and audio applications though recently they have started to penetrate into wireless communications area [29, 31]. On the other hand, sigma-delta interfaces are attractive for micro-machined inertial sensors since they combine the benefits of feedback and analog-to-digital conversion at a relatively modest circuit cost [9, 12, 27, 54].

The main goal in applying the $\Sigma\Delta$ modulation concept to inertial sensors is to achieve the benefits of feedback and digitization without compromising the resolution of the analog front end, as method for the design of a digital transducer. Therefore, the $\Sigma\Delta$

modulator should be designed such that the quantization error adds a negligible noise penalty. In additional to suppressing the noise from quantization the $\Sigma\Delta$ modulator loop must be compensated appropriately for stability.

The objectives of this work are:

1. To develop and examine $\Sigma\Delta$ modulators from both architectural and circuit level for implementation.
2. To identify both system and circuit level approaches.
3. To implement a $\Sigma\Delta$ modulator demonstrating the techniques developed in this work.

In the following sections, first overview of $\Sigma\Delta$ modulator based ADC's is given. Then a brief overview of Nyquist rate ADC's along with their limiting factors will be given. In Section 3.2, oversampling ADC's will be reviewed. Remaining sections of this chapter will be devoted to a special form of oversampling ADC's, namely delta-sigma ($\Sigma\ \Delta$) ADC. Section 3.3 will explain the operation principles and will describe performance metrics of delta-sigma ADC's. Various $\Sigma\Delta$ modulators (i.e. the analog part of a delta-sigma ADC) topologies will also be described in this section. Extensive system and circuit level simulations as well as experiments from a test prototype are presented in this chapter. Finally, some concluding remarks and future directions are given.

3.2 Principle Operation of Sigma-Delta Modulator

Analog-to-digital conversion is the process of converting a continuous in time and amplitude (analog) signal to a discrete in time and amplitude (digital) signal.

ADC's can be classified into two main categories according to the ratio of the sampling rate and the Nyquist rate. In Nyquist rate ADC's the sampling frequency is equal to the Nyquist rate. On the other hand, in oversampling ADC's the sampling operation is done at a much higher rate than the conversion rate. The ration of the sampling rate and the Nyquist rate is called oversampling ratio, M. ADC's can also be classified based on the main limiting factor of their resolution. All of Nyquist rate converters except the dual-slop converter fall in the category of ADC's that rely on component matching. Dual-slop and oversampling converters fall in the category of ADC's that rely on counting algorithm [29, 31].

3.2.1 Nyquist-rate Analog-to-Digital Converter

Nyquist-rate A/D converters can be subdivided into word-at-a-time, partial-word-at-a-time, bit-at-a-time, and level-at-a-time architectures depending on the number of bits that are quantized in a single clock cycle, thus the number of clock cycles needed to generate an output word. They all generally require an operation such as comparison, amplification or subtraction, be performed to the overall accuracy of the overall conversion. This typically translates into stringent demands on component matching over sub-circuits implementing them. Without some form of calibration or error correction in the manufacturing, it is difficult to deliver better than 12 bits of resolution [29, 31, and 55].

Also, Nyquist-rate ADC's use clock frequencies, which are not very high compared to the frequency of the processed signal. Nyquist-rate ADC's are used to digitize high-frequency and/or high-bandwidth signals. Since the frequency and/or

bandwidth of the processed signals are very high already, oversampling is often impractical. For the approach of high-resolution data converter, alternative architectures that do not require precise component matching is preferred. This research concentrates on oversampling ADC's, thus Nyquist-rate ADC's will not be discussed further.

3.2.2 Oversampling Analog-to-Digital Converter

Oversampling ADC's are based on trading off accuracy in amplitude for accuracy in time by combining sampling at well above the Nyquist rate with coarse quantization embedded within a feedback loop in order to suppress the amount of quantization noise appearing in the signal band. Unlike Nyquist-rate converters where each digital word is obtained from an accurately quantized single sample of the input, in oversampled converters, each output is obtained from a sequence of coarsely quantized input samples. The quantizer output is then used to generate higher resolution encoding of the signal. The use of feedback to attenuate the noise associated with the coarse quantizer is a critical aspect of oversampling A/D converters.

Unlike the Nyquist-rate converters, sampling is not a major problem for oversampling ADC's. Normally, dedicated sample/hold circuits are not required, because sampling is performed inherently by the circuits that perform quantization. Oversampling converters take advantage of today's VLSI technology tailed towards providing high-speed/high-density digital circuits rather than accurate analog circuits by performing most of the conversion process in digital domain [29, 31]. Analog part of these converters is relatively simple and occupies small area unlike their Nyquist-rate counterparts.

Oversampling ADC's can be classified into two main groups: straight-oversampling and noise-shaping ADC's. Straight-oversampling ADC's exploit the fact that the quantization noise is assumed to be uniformly distributed white noise over the entire frequency range. The higher the sampling frequency, the lower the quantization noise power per frequency. A major disadvantage of straight oversampling is that the accuracy speed trade-off is not efficient. In order to improve the resolution by 4-bit, the oversampling ratio must be increased by 256 times [31].On the other hand, the noise-shaping ADC's achieve a more efficient accuracy / speed trade-off by utilizing the noise-shaping concept in addition to oversampling. The noise- shaping is performed by placing the quantizer in the feedback loop in conjunction with a loop filter to reduce the quantization noise, which is created by converting an analog signal to a digital signal. The noise-shaping ADC employing a coarse quantizer is known as a sigma-delta ADC. Since the spectrum of the processed signal covers only a small fraction of the Nyquist bandwidth, the shaped noise can be filtered outside of the signal bandwidth in the digital domain. Oversampling, noise shaping, and filtering can result in exceptional accuracies. The bandwidth and/or frequency of the processed signal are not very high; however, it is well suited for the accelerometer interface design to achieve a high-resolution accuracy. In state-of-the-art oversampling ADC's, the oversampling ratio typically is between 8 and 256.

Shown in Figure 3.1 is a simple first-order, 1-bit ∑Δ modulator. This basic modulator is examined to explain the operation of a ∑Δ modulator. It comprises a discrete-time difference integrator and 1-bit quantizer that maps its input to both an analog and a digital output.

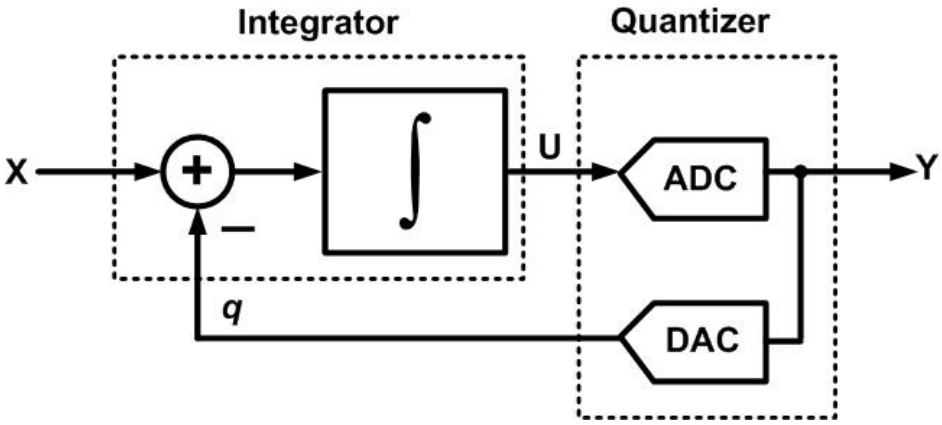


Figure 3.1: A first-order, 1-bit $\Sigma\Delta$ modulator.

The discrete-time difference integrator accumulates the difference between the input signal x[n], and the DAC output level, q[n], at its output, u[n]. When the integrator output, u[n], crosses the quantizer threshold, the sign of q[n] changes, reversing the polarity of the integrator input if |x[n]| < |q[n]|. This causes the integrator output to move in the opposite direction in the following cycle. Thus, the negative feedback loop tries to force q[n] equal to x[n]. However, the coarseness of the quantizer output causes q[n] to oscillate so that only its time average approaches x[n]. Therefore, the modulator output, y[n], is a digital bit stream whose average value is a digital approximation of the input signal.

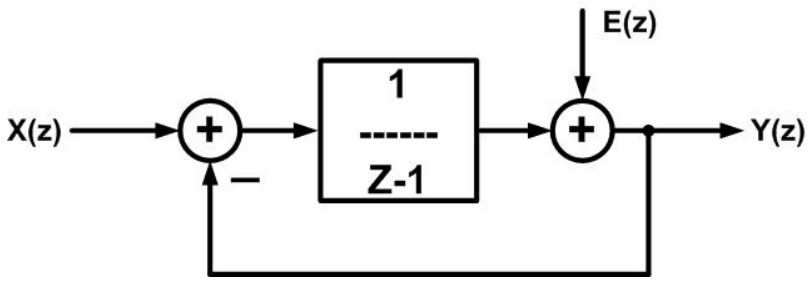


Figure 3.2: Linearized model of a first-order $\sum\Delta$ modulator.

By applying the white noise approximation, the modulator of Figure 3.1 may be represented by the linear system shown in Figure 3.2. The digital output of the modulator in z-domain can be derived as

$$Y(z) = z^{-1} \cdot X(z) + (1 - z^{-1}) \cdot Q_B(z) \tag{3-1}$$

One is the input signal delayed by one sample, the other is the quantization error filtered by a first-order difference, which has the transfer function $H_Q(z)=1-Z^{-1}$. This filtering, referred to as noise shaping, places a zero at dc, thereby attenuating the low-frequency quantization noise.

The first-order $\Sigma\Delta$ modulator can be extended to a higher-order noise shaping modulator by inserting more integrators to the feed-forward path of the modulator. Assuming same delaying integrator, L is the order of filter loops, the transfer function of an L^{th}-order noise shaping modulator may be derived as

$$NTF_B = (1 - z^{-1})^L \tag{3-2}$$

This noise transfer function has L zeros at DC, resulting in L^{th}-order noise shaping.

3.2.3 The Sigma-Delta Modulator

While there are many ways of implementing a force-feedback accelerometer closed-loop, a sigma-delta modulator used as an oversampling ADC is particularly attractive because it has a relatively simple structure, provides digital output with a large bandwidth, and is easily implemented in CMOS technologies [10, 29].

Sigma-Delta modulators can be roughly categorized into the following types: low-order single-bit single-loop, high-order single-bit single-loop, single-bit multi-loop

(cascaded or MASH), and multi-bit (single-loop or multi-loop). Each topology has its own share of advantages and disadvantages, as they will be discussed thereafter.

In order to achieve a large signal-to-noise-ratio (SNR) and high-resolution in one sigma-delta ADC circuit, adopting a higher-order structure is inevitable [29]. In reality, a sigma-delta ADC is a highly nonlinear circuit. When more than two integrators are cascaded in the sigma-delta modulator loop, it becomes prone to instability when the modulator is excited by a large input signal.

3.2.3.1 Cascaded ∑Δ (MASH) Modulator

An alternative method of implementing a higher-order sigma-delta modulator is to cascade multiple lower-order stages in such a way that each stage processes the quantization noise of the previous stages. It is commonly called the multi-stage (MASH) modulator. The quantization noise of all stages, except the last stage, is removed and the last stage quantization noise is high-pass filtered by the noise transfer function [29, 33]. For such a structure, the output noise is extremely low if the proper transfer functions are well controlled. The maximum input range is almost equal to the reference voltage level, and a high SNR for a given oversampling ratio can be achieved. Theoretically they offer good performance, but they require nearly perfect matching between analog and digital blocks. And complex SC circuits are required to ensure matching [56]. However, the stability and the performance are very sensitive to the nonidealities of the first stage and mismatches, which can result in a serious deterioration of the noise performance of the converter.

For example, the noise-shaping performance is that of a 4th-order single-loop converter shown in Figure 3.3, while the stability is that of a 2nd-order one, assuming both internal feedback loops are order of 2.

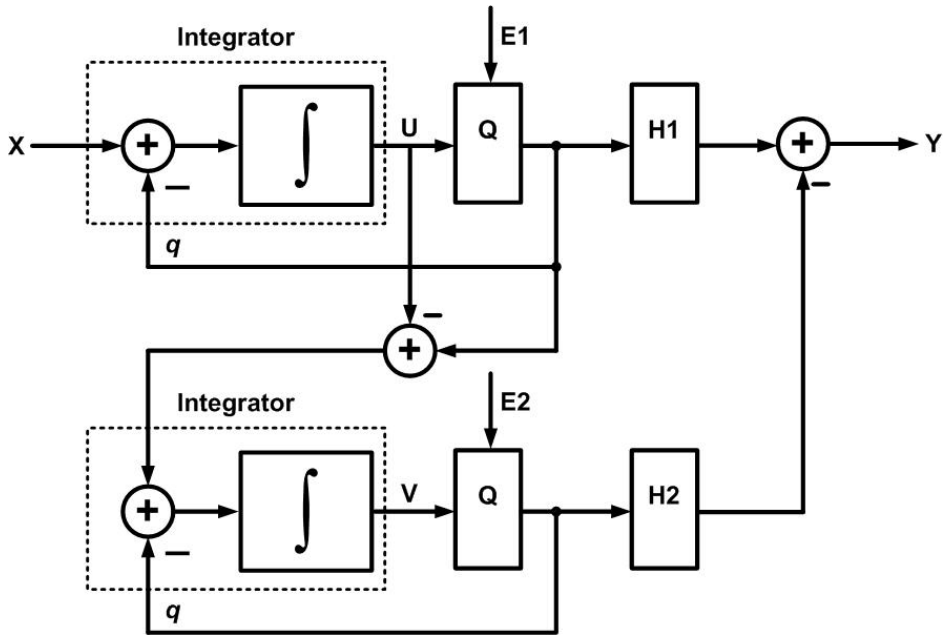


Figure 3.3: Diagram of a MASH architecture.

The overall output of the modulator in Figure 3.3 is

$$Y(z) = z^{-4} \cdot X(z) - (1 - z^{-1})^4 \cdot E_2(z) \tag{3-3}$$

Assuming the following condition is met

$$H_1 \cdot NTF_1 - H_2 \cdot STF_2 = 0 \tag{3-4}$$

Due to imperfections in the realization of the analog transfer function, noise E1 will appear at the output. This may result in serious deterioration of the noise performance of the converter. The exact noise cancellation depends on the matching of the two loops and

the precision of the ADC in the cancellation loop. In real circuit implementation, the mismatches of the loop coefficients, the finite OTA dc gain and the settling error of the integrator result in the noise leakage into the baseband and serious deterioration of the noise performance. All these make the implementation difficult [57-58].

3.2.3.2 Single-loop High-order $\sum\Delta$ Modulator

For a single-loop lower-order 1-bit modulator, it has guaranteed stability. The loop filter design and circuit implementation is easy, but they are more prone to idling tones in the baseband than higher-order 1-bit modulator, thus do not achieve high SNR.

Increasing the number of bits in the quantizer increases the SNR of modulator significantly. For each additional bit in the quantizer, the SNR of the converter increases by 6dB. Moreover, the loop stability can also be improved and loop coefficients can be enlarged. The more powerful noise shaping ability is obtained [29]. Multi-bit is normally used for high-frequency signal. Generally speaking, the multi-bit modulator offers the best performance in increased SNR and better stability (the modulator behaves closer to the linearized theory, fewer spectral tones), but suffers from the nonlinearity problems of the feedback DAC. However, the linearity of the multi-bit DAC in the feedback loop directly affects the linearity of the converter. Since the feedback loop is connected to the input of the converter, any nonlinearity in the DAC can not be distinguished from the input signal and will leaked at the output, thus directly affect the modulator's performance, and ultimately, limit the modulator's SNR. Therefore, the accuracy of the DAC should be at least as good as the $\sum\Delta$ modulator in order not to degrade the

performance of the $\Sigma\Delta$ modulator, which lead to the need for auto-calibration or dynamic element matching techniques at the cost of even more complex add-on circuits with DAC design [58-62]. The use of multi-bit quantizers and DAC error correction increases the complexity of the circuitry and hence more chip area and power budget.

For the intrinsic linearity of the single-bit quantizer and the inherently linearity of the 1-bit feedback DAC, many $\Sigma\Delta$ ADC's employ the single-bit quantizer. They are less prone to idle tones. Thus, a high-order single-bit single-loop delta-sigma modulator is in favor in this research work because of its advantages shown in Table 3.1. Many approaches have been devised to implement stable, higher-order, single-stage, 1-bit $\sum\Delta$ modulation [63-66]. Nevertheless, a high-order single-bit single-loop modulator doesn't unconditionally guarantee stability. Stability is signal dependent. The maximum input range must be restricted to ensure stability [57]. Appropriate zeros can be introduced in the loop filter at the expense of some additional circuit complexity to stabilize the modulator for a certain input range.

TABLE 3.1: COMPARISONS OF MODULATOR TYPES

Modulator Type	SNR vs. OSR	Linearity	Circuit design Simplicity	Stability Issues
Low-order 1-bit single-loop	×	×	√	√
High-order 1-bit single-loop	√	√	√	×
1-bit multi-loop (cascaded)	√	×	×	√
Multi-bit cascaded	√	×	×	√

After a methodology is established for stabilizing higher-order single-loop $\Sigma\Delta$ modulators [67-71], several versions of loop filters, and therefore modulators can be designed. Most commonly used higher-order modulators are the so called distributed feedback (DFB) [72-73] and distributed feedforward (DFF) [74-77] type modulators depicted in Figure 3.4.

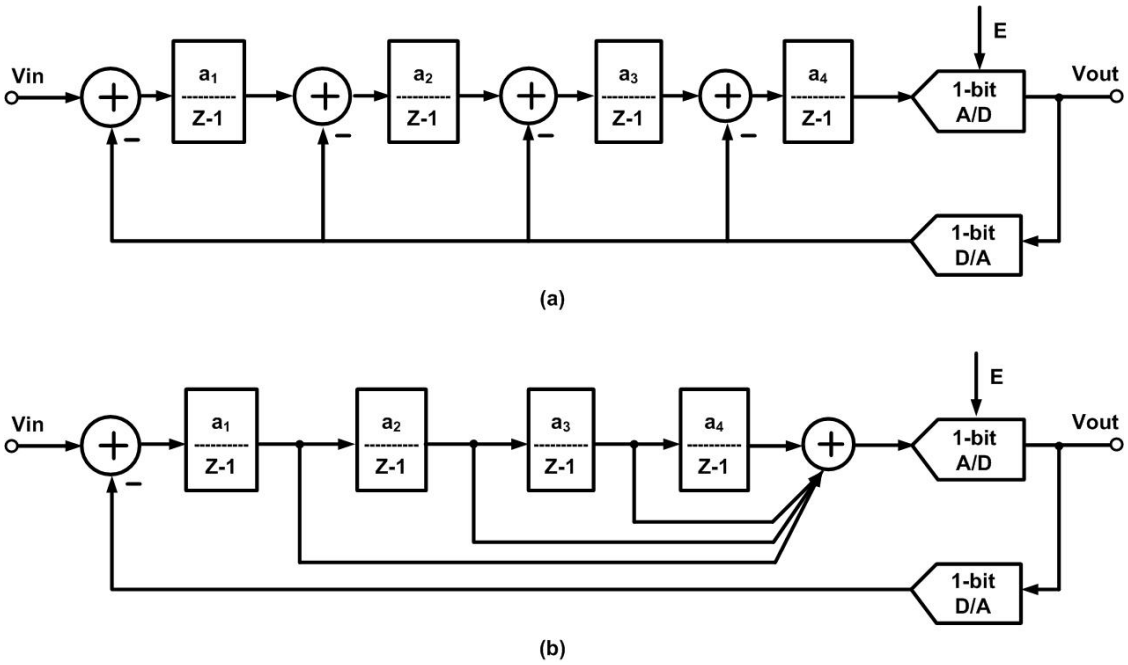


Figure 3.4: (a) A 4th-order DFB modulator, and (b) a 4th-order DFF modulator.

And there are many other loops possible. Multiple methodologies have been developed in the past to improve the sigma-delta modulator's stability condition. The mixed structure combining DFB and DFF is based on cascaded integrators with feedback branches to position the poles and feed-forward branches to position the zeros. It provides the proper SNR performance and flexible stability control through these coefficients. However, these structures are complicated. The exact coefficient positioning is difficult to maintain in the real circuit implementation.

3.3 SYSTEM DESIGN OF THE ADC

In this section, a baseband fourth-order single-loop 1-bit sigma-delta modulator intended for accelerometer applications is introduced; whose signal bandwidth requirement is less than 100 Hz. The typical sigma-delta ADC has a resolution in the range of 12-16 bits with signal bandwidths from 20 KHz to 5 MHz [29].

First, an architectural overview of the proposed modulator is given. Then the system level simulations from Matlab are presented.

3.3.1 Modulator Architecture

The block diagram of the proposed fourth-order modulator is depicted in Figure 3.5. The modulator has a mixed loop topology having both feedback and resonator paths. This structure is developed to explore the maximum stability and also to achieve a high performance in practice. No active summing element is required, thus only four op amps are necessary as it would be in DFB architecture. The gain coefficient of the first integrator can be large while keeping the integrator output swing low similar to the case of DFB architectures.

The loop coefficients a's, c's and g's --- determine the pole locations of the noise transfer function whereas c's and g's determine the position of the complex zero pair. The remaining zeros are at DC. The poles are distributed through the signal band in order to lower the in-band noise. The zeros are chosen to flatten the filter response at high frequency in order to reduce the high-freq noise and prevent if from using up the dynamic

range. The feedback around the last two integrators forms a resonator. By the proper choice of the feedback factor a, the complex zeros can be situated to give optimum noise suppression in the baseband. The resonators in modulator generate complex pairs of zeros. This allows the placement of zeros on the unit circle at finite positive frequencies, allowing the NTF magnitude response to exhibit one or more notches in its frequency response. Better SNR will be achieved. Thus further reduce the in-band mean value of NTF and suppress the total in-band quantization noise. All the integrators have one unit delay for fast settling.

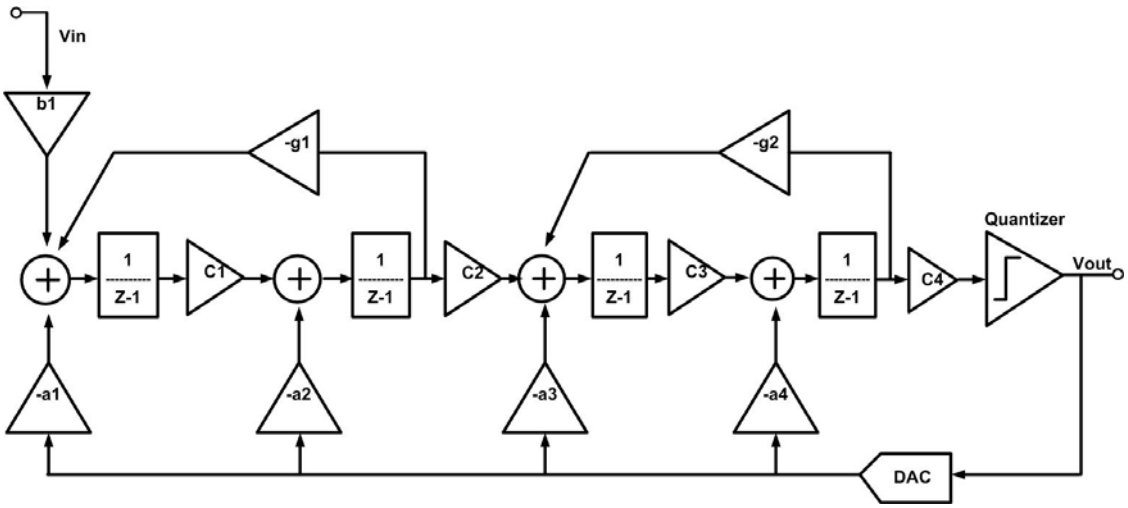


Figure 3.5: The function block diagram of the proposed 4th-order modulator.

The overall z-domain transfer function of the system can be written in terms of the input signal X(z), quantization noise E(z), and the signal and noise transfer functions, STF(z), and NTF(z), respectively.

$$Y(z) = STF(z)\,X(z) + NTF(z)\,E(z) \qquad (3\text{-}5)$$

With

$$SNT(z) = \frac{0.0061273}{(z^2 - 1.492 \cdot z + 0.5646)(z^2 - 1.702 \cdot z + 0.787)} \tag{3-6}$$

and

$$NTF(z) = \frac{(z^2 - 2 \cdot z + 1)(z^2 - 2 \cdot z + 1)}{(z^2 - 1.492 \cdot z + 0.5646)(z^2 - 1.702 \cdot z + 0.787)} \tag{3-7}$$

Note that the high frequency gain of the NTF is close to 3dB, which is necessary for stable modulator design [29, 78].

Clearly, the above description of the modulator is based on a linear model. Such a linearized model may lead serious modeling errors especially for higher-order modulators [29, 78]. As mentioned in 3.1, the highly nonlinear nature of the single-bit quantizer invalidates the linearized model. However, modeling the nonlinear system at hand as a linear system with the single-bit quantizer (i.e., the comparator) as a linear gain element facilitates the study of the system at hand [58, 65].

3.3.2 System Level Simulations

MATLAB routines have been extensively used to describe the $\Sigma\Delta$ modulator behavior and post-process the modulator output bit-stream.

The simulations can be grouped into two parts. 1) Time domain simulations for determining the stable input range and integrator output swings. Based on the results, the loop coefficients are chosen to give a large input range and integrator gains are adjusted to limit integrator output swings. 2) Frequency domain simulations for determining various performance metrics (such as SNR and DR) of the modulator, including the

effects of circuit nonidealities. The simulation data are utilized to determine amplifier specifications.

If integrator output swings are larger than a certain level, say for example the output swing of a particular amplifier or the supply voltages, the modulator loop coefficients have to be adjusted in order to scale down the integrator output swings. Finally when all the loop coefficients are adjusted, it becomes a different task to choose the capacitor sizes to be used in modulator realization in real circuit implementation. So the main design goals are to relax critical analog circuit design requirements with architectural level solutions and to enable area/power efficient design in CMOS digital process.

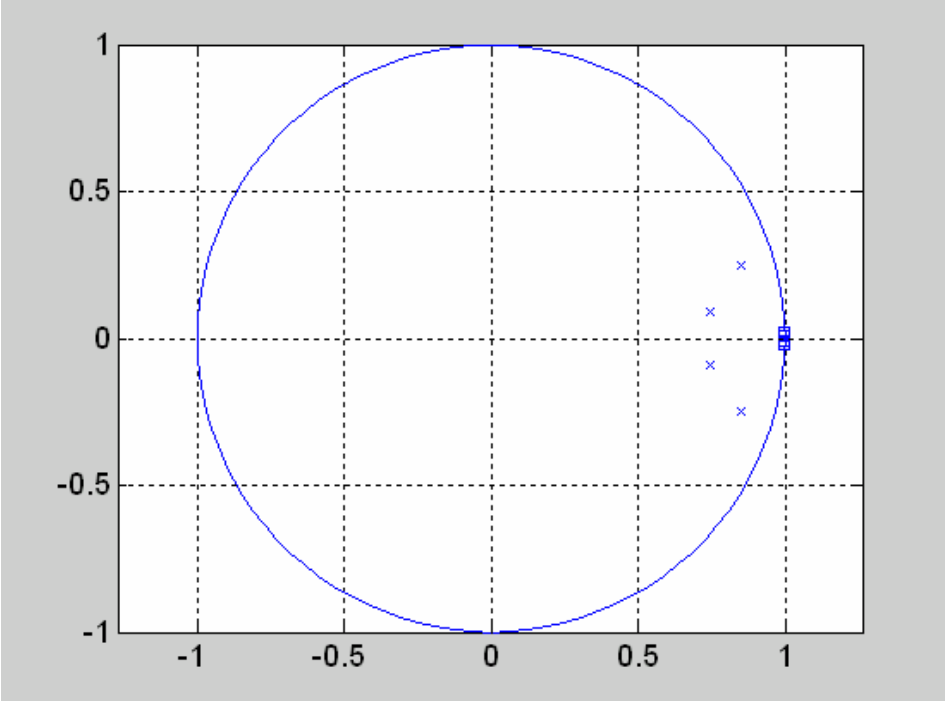


Figure 3.6: Poles and Zeros of NTF.

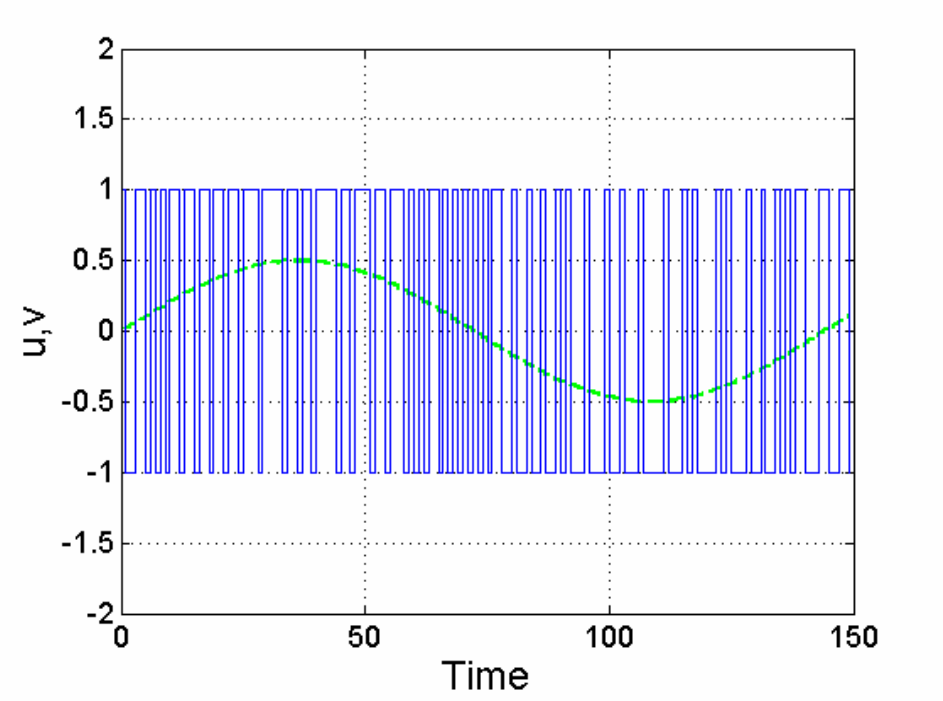


Figure 3.7: Simulated Input vs. Output of the modulator.

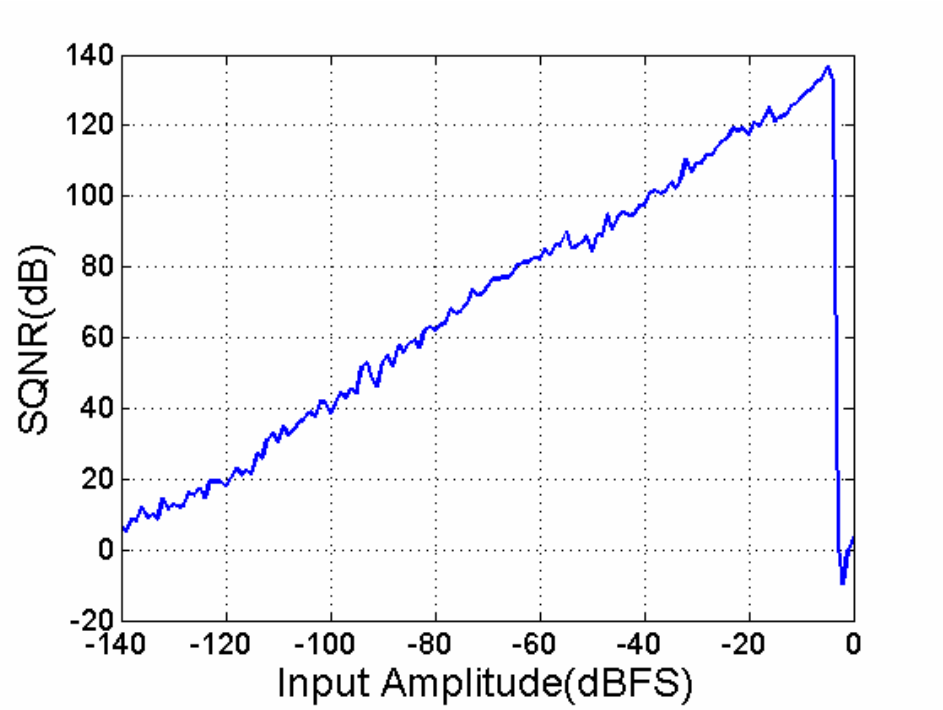


Figure 3.8: Simulated DR vs. different input amplitude.

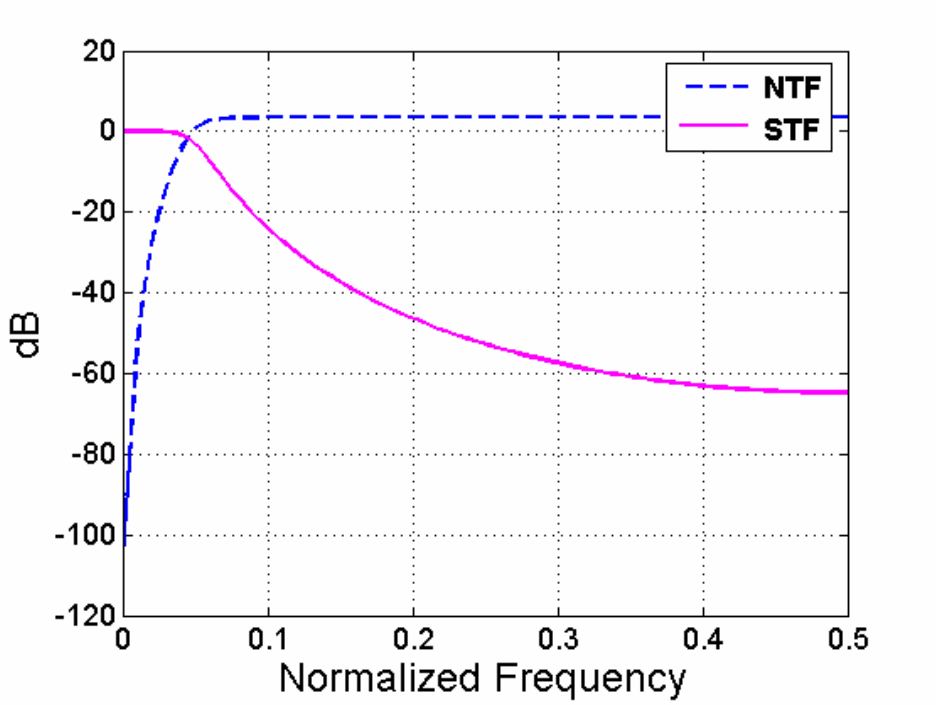


Figure 3.9: Simulated STF and NTF of the designed system.

3.4 Circuit Implementation and Layout Consideration

At architecture level, the SC circuits are the most often used in a $\Sigma\Delta$ ADC's, they are better suited for high-linearity integrators, and offer better stability (higher overloading levels for the same NTF aggressiveness) and easier timing of quantizer and DAC signals inside the loop. Also, Switched capacitor techniques are employed to implement the analog sub-circuits mainly because of their high immunity to clock jitter effects. They are also less sensitive to circuit non-idealities than the continuous time (CT) counterparts. On the other hand, CT integrators are more prone to clock jitter and demand stringent settling requirements. In additions, in SC integrator, variation in gain factor depends on the relative accuracy of components (ratio of two capacitors) rather than the

absolute value of components (either RC-product or gm/C ratio), therefore it is well controlled. In a standard CMOS process, the mismatch error of on-chip capacitors can be less than 0.1% for good layout. As a consequence, SC systems guarantee very accurate frequency response without component trimming. Due to several drawbacks of continuous time integrators for high-resolution $\Sigma\Delta$ modulators, SC integrators have been favored more than CT counterparts.

3.4.1 Circuit Implementation

The modulator is realized a in 0.6um n-well CMOS technology with three metal layers by adopting a fully-differential SC implementation. The fully-differential architecture doubles the signal swing and increases the dynamic range by 3dB. Moreover, the common-mode signals which may couple to the signal through the supply lines and the substrate are rejected and charges injected by switches are canceled to the first order. The modulator is fully pipelined by realizing all the integrators with one sample delay. This prevents the double-settling problem in which two series connected op amps have to settle in one clock period. Such a case demands faster op amps, resulting in high power consumption. A two-phase non-overlapping clocking scheme is adopted in order to minimize signal dependent charge injection, which are generated externally.

Figure 3.10 shows the SC-implementation of the 4^{th}-order $\Sigma\Delta$ ADC. The size of sampling capacitor of the first integrator is determined by KT/MC noise limitations rather than matching requirements. Capacitor values have also been included in the Table 3.2.

In this higher-order $\Sigma\Delta$ ADC, the additional integrators randomize the quantization error and thus whiten the quantization noise spectrum. In hardware

implementation, the inevitably additional noise sources such as Brownian noise from the sensing element and electronic noise from the interface electronics, these act as a dither signal and further suppress the tone behavior due to limit cycles. Also, the reduction of the dead zone in a higher order ADC is due to the additional electronic integrator in the forward path, which has greater gain at low frequencies. So, for most practical considerations the effect of a dead zone can be neglected. The dithering circuit is not added in the system.

TABLE 3.2: COEFFICENTS TABLE

Coefficients	Calculated	Implemented	Cap value
a1	0.09448	0.1	1pF/10pF
a2	0.17424	0.175	350fF (2×100f+150f)
a3	0.2654	0.265	530fF (4×100f +130f)
a4	0.27299	0.27	540fF (4×100f+140f)
b1	0.094485	0.1	
C1	0.1746	0.175	350fF
C2	0.31982	0.32	640fF (5×100f+140f)
C3	0.39213	0.4	780fF (6×100f+180f)
C4	2.96	Not implemented	Ignored in design
g1	0.0003987	0.0004	Capacitive-T network
g2	0.001139	0.001	Capacitive-T network

Notes:

The rest “b” coefficients are set to zero.

100fF and 1pF are unit capacitor cells used in the design.

In high resolution $\Sigma\Delta$ modulators, the low-frequency noise such as flicker noise of the op amp may limit the DR. The low-frequency noise can be reduced by the double-correlated-sampling (CDS), or chopper stabilization techniques. Low frequency noise of

the MOS device causes undesirable drift and degrades the stability of the data converter. Chopper stabilization at the system level can reduce the circuit noise more efficiently [79]. It consists of placing one SC mixer for frequency fs/2 at the op-amp input and a similar one at the opamp output. This action does not affect white noise. On the other hand, offset and 1/f noise are shifted to around fs/2, not affecting the frequencies around dc, where the signal to be processed is supposed to be. In terms of power dissipation and non-linearity reduction, the best time for chopping is at the beginning of the sampling (reset) phase.

For op-amp used in integrator, finite SR and DC gain variations with respect to the output voltage are the two main nonlinearity sources. Unlike the CT circuits, slewing is most often unavoidable for SC circuits for normal input signal levels.

The op-amp used in chopper stabilized integrator must have better settling characteristics than a regular integrator. This is because, during chopping the polarity of the integrator output is reversed, hence the amplifier output must change one output extreme to the other.

A typical class-AB amplifier requires two stages: a static-biased input stage and a class-AB output stage. A two stage class-AB differential amplifier may need two common-mode feedback control circuit [80], which makes it more power hungry and/or more complex, which are suitable for a restrict power budget. Therefore, for high performance designs the class-A op-amp is selected in our design, while class AB op-amps are suitable for those with a restricted power budget.

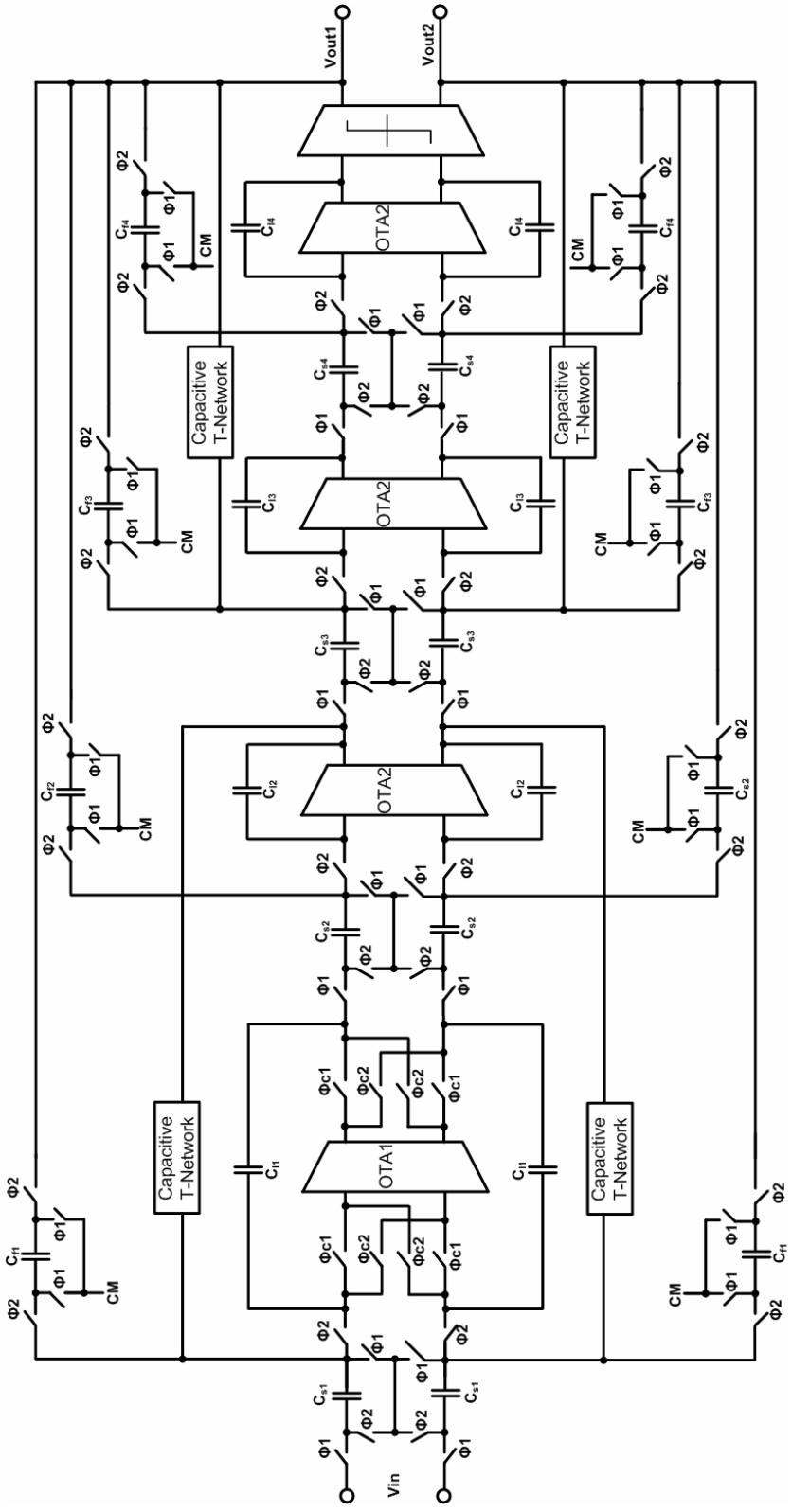


Figure 3.10: Schematic diagram of the 4th-order ∑Δ modulator.

For the op-amp noise, the noise band is usually correlated with the signal bandwidth. Therefore, a good op-amp settling (achieved with a large signal bandwidth) is in contrast to low-noise performance (achieved with reduced noise bandwidth). Therefore, in low-noise systems, the bandwidth of the op-amp is designed to be the minimum that guarantees proper settling. The SC CMFD is not used, because the additional switching load present at the output of the amplifier, which is important in fast-settling, low-distortion SC integrators.

Note that, in an integrator which does not employ chopper stabilization, in sampling phase the amplifier has to charge only the sampling capacitor of the following SC-stage, therefore, normally settling requirements in sampling phase is very relaxed compared to the chopper stabilized integrator. So the OTA designed for the capacitive amplifier at the front interface, which is described in detail at Chapter 2, will be used again in these integrators.

The comparator in a sigma-delta modulator serves as a one bit quantizer and generates a stream of digital outputs. In the linearized delta-sigma model, an ideal comparator is replaced by an additive white noise source. The intrinsic offset voltage and device noise of a practical comparator can be treated as an additive noise superimposed on the quantization white noise [67, 81]. The comparator hysteresis can also be modeled as additive white noise. Therefore, all the nonidealities of the comparator experience the same noise-shaping as the quantization noise. This means that the nonidealities of the comparator within the signal bandwidth are reduced. This put less stringent requirement on the comparator design.

The single-bit quantizer is realized by using a preamplifier, a dynamic comparator, and a D-latch/SR-latch, as show in Figure 3.11. The preamplifier is used to obtain higher resolution and to minimize the effect of kickback. The latched comparator is rest at each clock cycle to enable high speed operation. This combines the best aspects of circuits with a negative exponential response (the preamplifier) with circuits with a positive exponential response (the latch) [81].The last stage is a SR-latch which is added to obtain the output signal in memory [78]. Bias current and transistor size are optimized to meet the speed requirements, while injecting the lease amount of noise into the substrate.

Figure 3.11 shows the regenerative comparator used in the system. The comparator offers benefits of high speed, low power and small area. Many several of these simple latch type comparators are widely used in $\Sigma\Delta$ modulators. Transistor M7, M8 and M11 form a pull-up positive feedback latch while transistors M9, M10, and M12 form a pull-down positive feedback latch.

When the latch signal is low, the differential outputs are reset to Vdd. As the latch signal turns high, the output of the cross-coupled inverters flips in the appropriate direction according to the input signal scale. The output of dynamic latch is stored in a SR latch that is implemented with CMOS NOR gates. Inverters buffer the outputs of the SR latch used in the comparators that drive NMOS switches connected to the negative reference voltage and PMOS switches connected to the positive reference voltage. The comparator offset is lower than 5mV and hysteresis is no more than 10ns, which is sufficient for the application. The simulation result is shown in Figure 3.12.

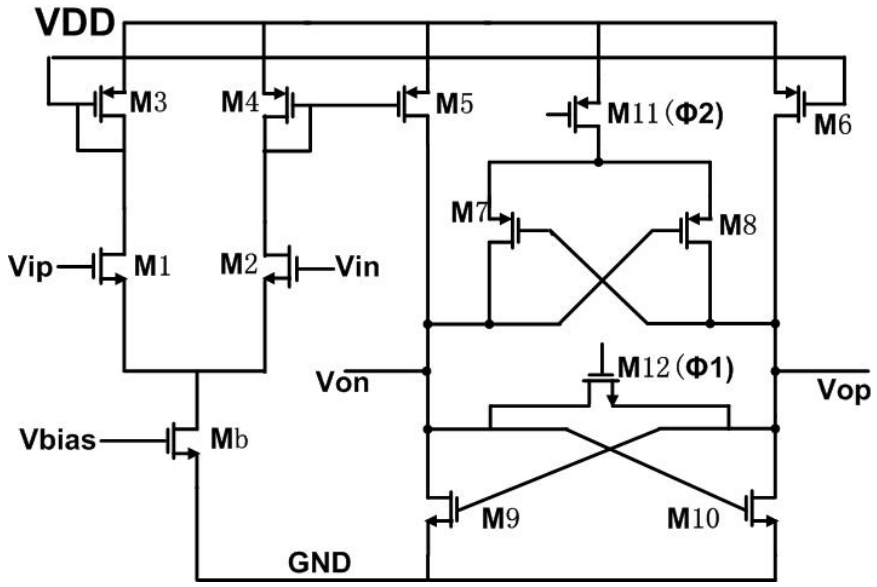


Figure 3.11: Schematic diagram of the comparator.

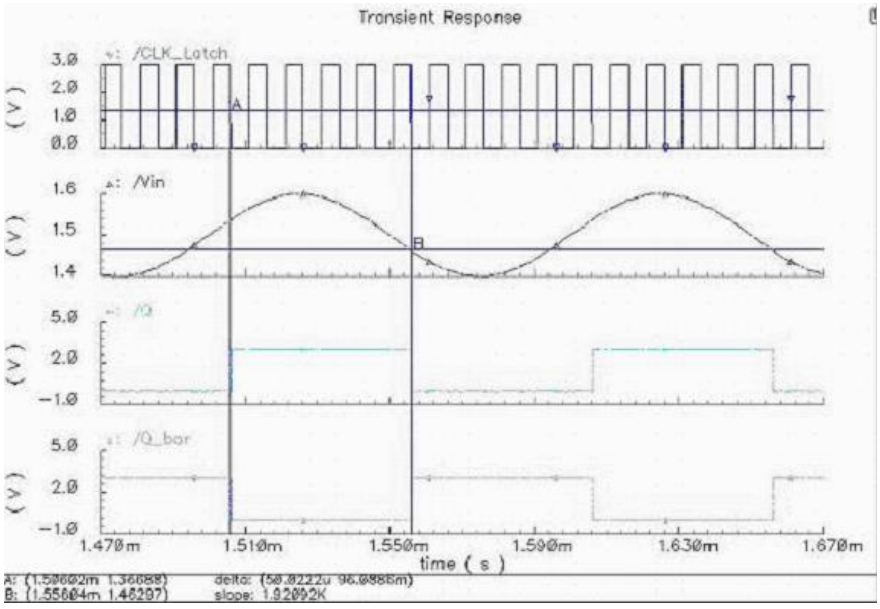


Figure 3.12: Comparator simulation result.

In the design of first stage integrator, as show from the Table X, the pole frequency fp is very low with respect to the sampling frequency fs, then the capacitor

spread S = C_f/C_s of a standard integrator will be very large. This causes a large die area and reduced performance accuracy for poor matching.

One solution to reduce the capacitor spreading is based on the use of a capacitive T-network in a standard SC integrator, as shown in Figure 3.13. The operation of the sampling T-structure is to realize a passive charge partition with the capacitors C_{s1}, and C_{s2}+C_{s3}. The final result is that only the charge on C_{s3} is injected into the virtual ground. Therefore, the effect of this scheme is that C_s is replaced with the C_{s_eq}, given by the expression:

$$C_{s\_eq} = C_{s3} \cdot \frac{C_{s1}}{C_{s1} + C_{s2} + C_{s3}} \tag{3-8}$$

The net gain of this approach is that, using proper ratio among C_{s1}, C_{s2}, and C_{s3}, the capacitor spread can be reduced. For example, an integrator with C_s = 1 and C_f= 40, can be realized with C_{s1} = 1, C_{s2} = 6, C_{s3} = 1, and C_f = 5, i.e., with the capacitor spread reduced to 6.

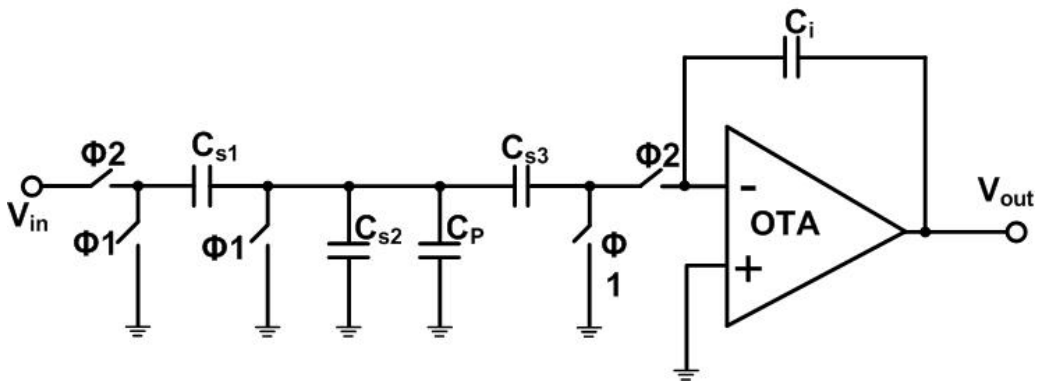


Figure 3.13: Capacitive T-network configuration.

$$\frac{V_o}{V_i} = \frac{C_{s1}}{C_{s1} + C_{s2} + C_{s3}} \cdot \frac{C_{s3}}{C_i} \cdot \frac{1}{1 - Z^{-1}} \tag{3-9}$$

The problem of the circuit of Figure 3.13 is due to the fact that the T-network is sensitive to the parasitic capacitance C_p (due to C_{s1}, C_{s2}, and C_{s3}) in the middle node of the T-network, which is added to C_{s2}, reducing frequency response accuracy.

3.4.2 Final Layout Consideration

The floor plan of the proposed modulator is depicted in Figure 3.14. Amplifiers are laid out using well-known techniques to improve matching; where matching is crucial, common-centeroid layout is used. When it is less critical, transistor pairs are laid out within close proximity without employing cross-coupling. All the capacitors and dummy capacitors are laid out using unit capacitors in order to improve matching. For the first stage, the unit capacitor is 1pF, whereas for the remaining stages the unit capacitance is l00 fF for the rest stages.

In the layout, amplifiers, capacitors, switches, and clock and analog signal lines are put in separate areas for die area efficiency and to isolate analog signal lines from the clock and other digital lines.

The top portion of the layout is devoted to analog power, ground, reference, and bias lines. The area underneath is for amplifiers with bias circuits. The bias generator is placed approximately in the middle of the layout. The area below amplifiers is for capacitors. Analog signal lines are placed between the capacitors and switches. The area below the switches is for the clock bus, the clock generator, the quantizer, and ground lines.

In order to minimize parasitics the following techniques are used. All signal lines made as short as possible and when possible, routed in metal 2 rather than metal 1. Resistance of power and ground and critical signal lines are lowered by routing them entirely in metal. Analog and digital parts are laid further apart for good isolation. Capacitors (including dummy capacitors) are placed in a well whose potential is tied to a ground line to minimize substrate noise pickup.

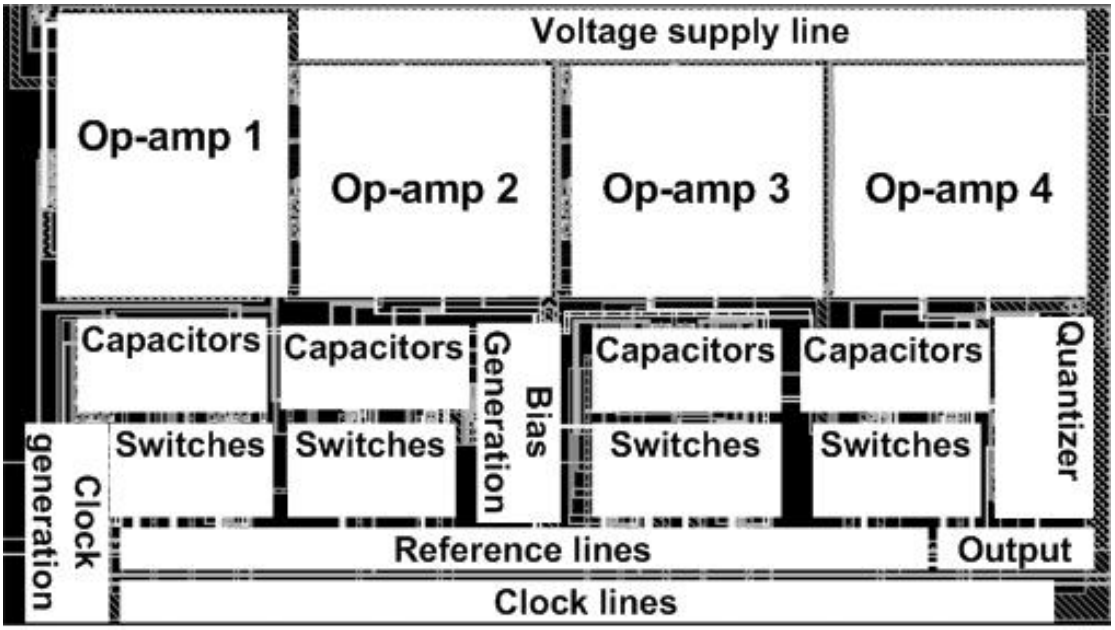


Figure 3.14: Floor plan of the modulator.

3.5 Measurements

Measurement results from an experimental prototype integrated in a 0.6μm CMOS technology from AMI is presented in this section. However, since the measurement setup is highly crucial in determining the performance of a high-resolution

ADC it is worthwhile to describe the test environment prior to presentation of the experimental results.

Also, for the low-frequency noise performance, the optimized lateral BJT devices are introduced in this 0.6μm process in the 1st stage of integrator of the ADC. The same techniques tThe test results are shown in this section too.

Finally, the accelerometer device is wire-bonded to the front-end read-out circuit and back-end ADC circuit to test the functionality.

3.5.1 Measurement Setup

The differential input signal to the modulator, generated by Tektronix AFG 3102, is directly applied to the modulator.

Modulator outputs are buffered by a series of on-chip inverters before they are transferred to the data acquisition system --- Agilent dynamic signal analyzer.

The test board is implemented using a 2-layer printed circuit board (PCB).

3.5.2 Results

For oversampled ADC, since the operation principles are different from the Nyquist ADC's, different performance metrics are used to evaluate the performance. In Figure 3.15, with the sampling clock at 50KHz, the pulse-width-modulated bit stream at the output is verified for the input sine wave of 1V (pk-pk) at 100Hz bandwidth. In Figure 3.16, at the maximum high of the input, more output bits stay at logic high. In Figure 3.17, more output bits stay at logic low when at the maximum low of the input. At

the zero-crossing point of the input, the output has certain delay, which is shown in Figure 3.18.

Because of the overloading effect, DR cannot be used to define the effective number of bits (ENOB) since the full input scale is not at 0dBR. From Figure 3.18, the 4^{th}-order noise-shaping factor is presented with 80dB/dec slop in the power spectral density plot. In the same time, DR does not explicitly include non-linearity information. The SNDR is used to approximately calculate the ENOB as

$$ENOB = \frac{(PeakSNDR) - 1.76}{6.02} \approx \frac{PeakSNDR}{6} \tag{3-10}$$

The DR extracted is about 65dB measured at 10Hz signal bandwidth, as show in Figure 3.20.

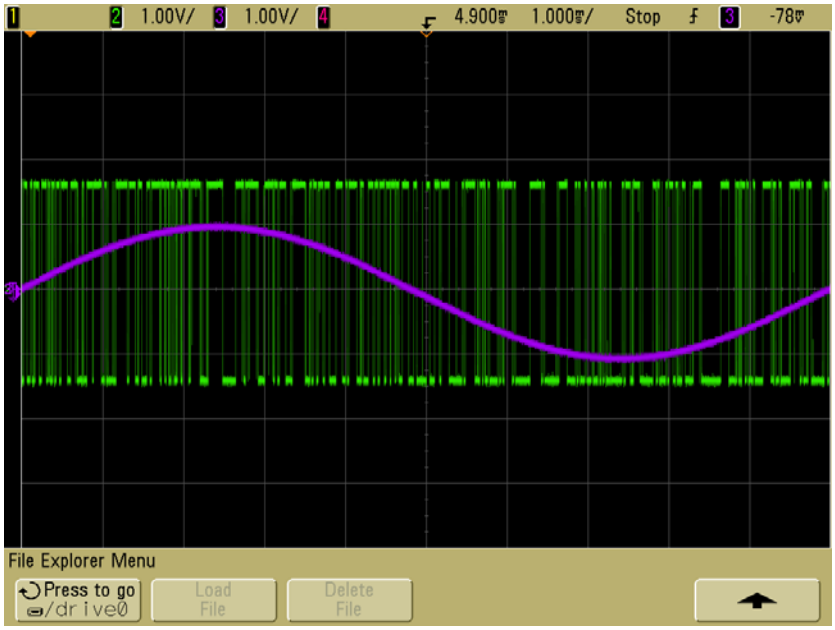


Figure 3.15: Input vs. output of modulator with fs=50Khz & fb= 100Hz @1Vpk-pk.

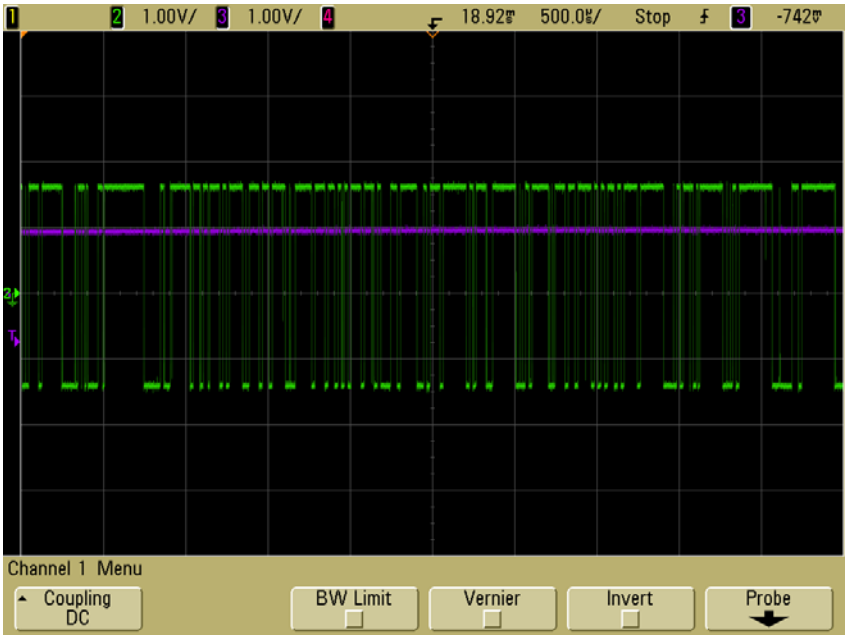


Figure 3.16: Output of the modulator at max input high.

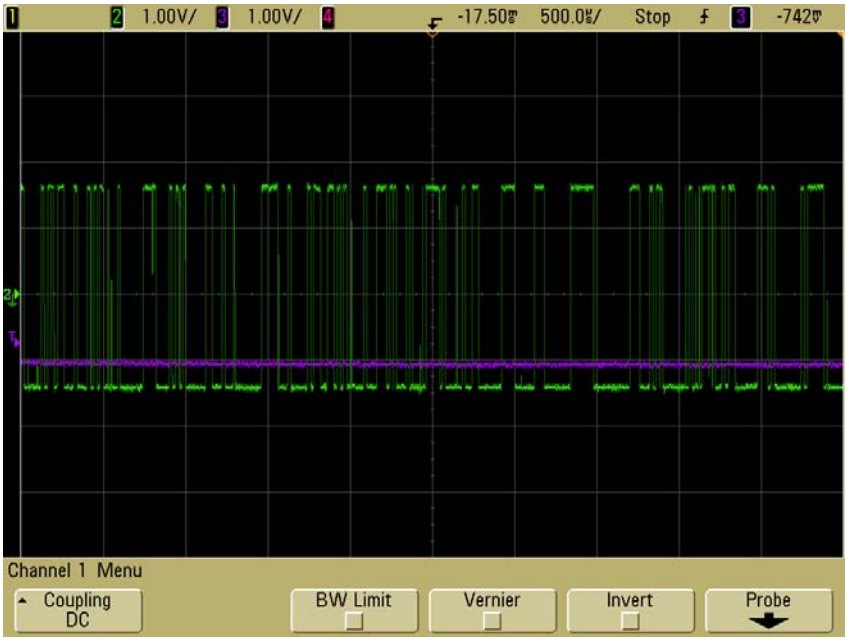


Figure 3.17: Output of the modulator at max input low.

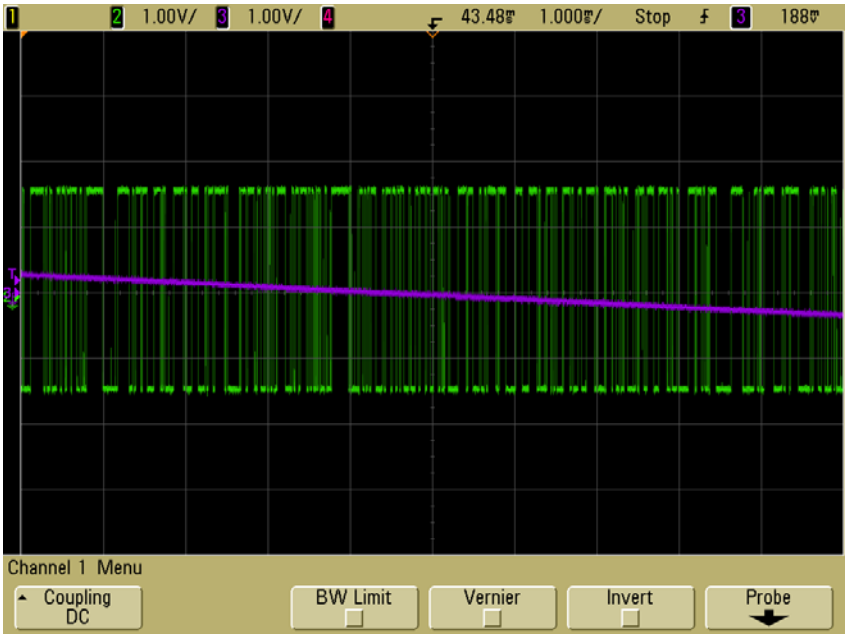


Figure 3.18: Output of the modulator at zero-crossing point.

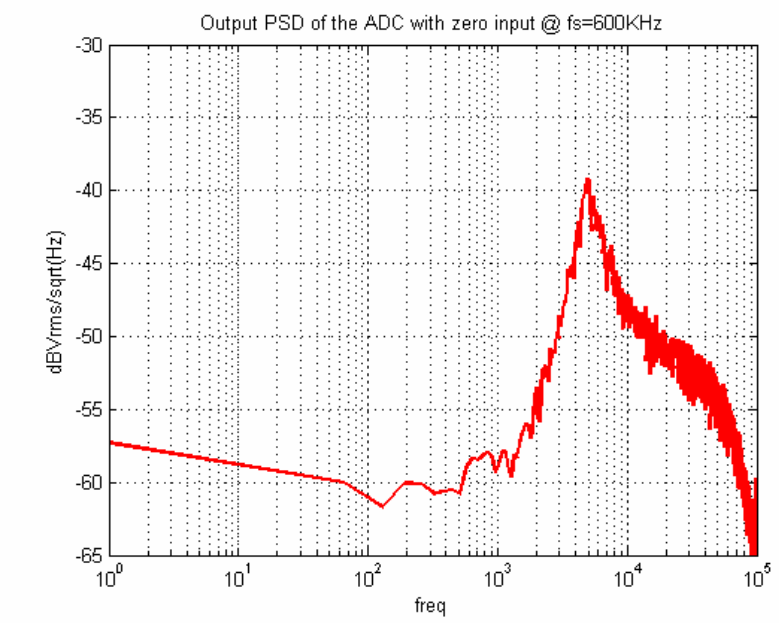


Figure 3.19: Output noise PSD of the modulator.

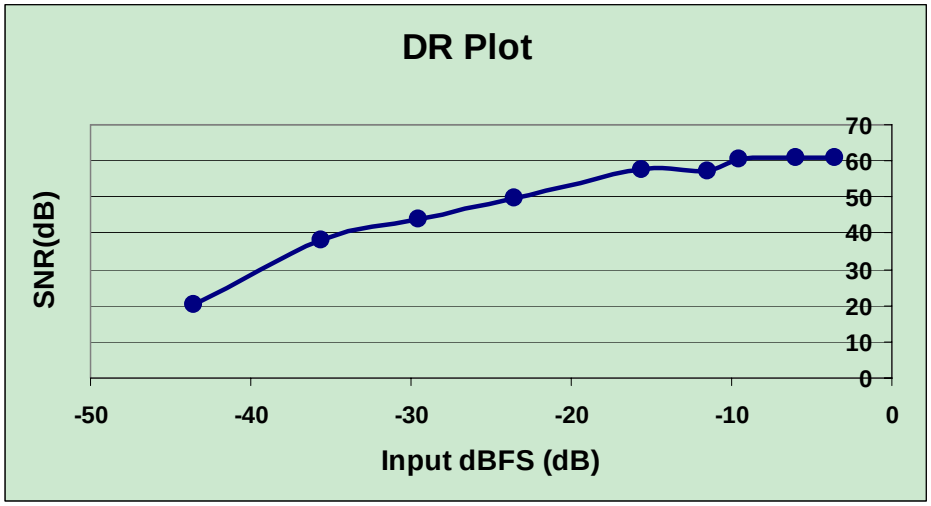


Figure 3.20: Extracted 65 dB DR vs. different input amplitude at 10 Hz bandwidth.

The IC die picture is shown Figure 3.21. The size is 1.5 mm × 3 mm.

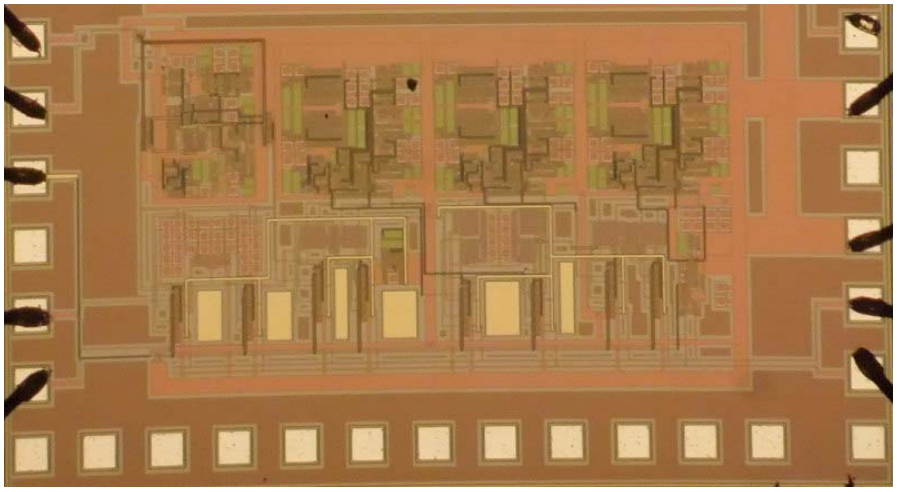


Figure 3.21: The micrograph of IC die made from AMI 0.6 μm process.

With the lateral BJT implementation inside the 4th-order ADC, these circuits showed the compatible performance.

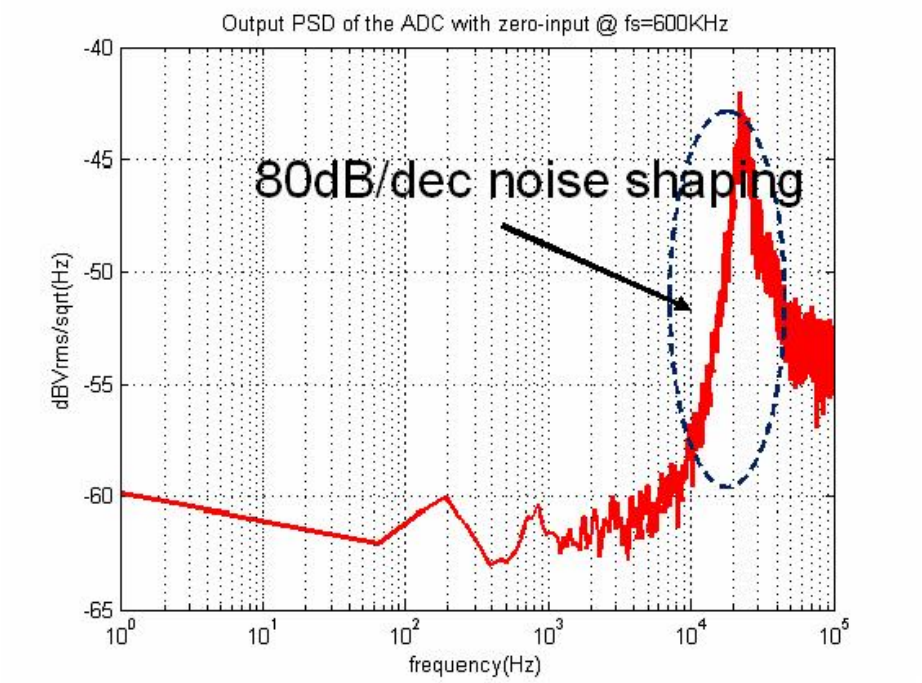


Figure 3.22: Output noise PSD of the modulator.

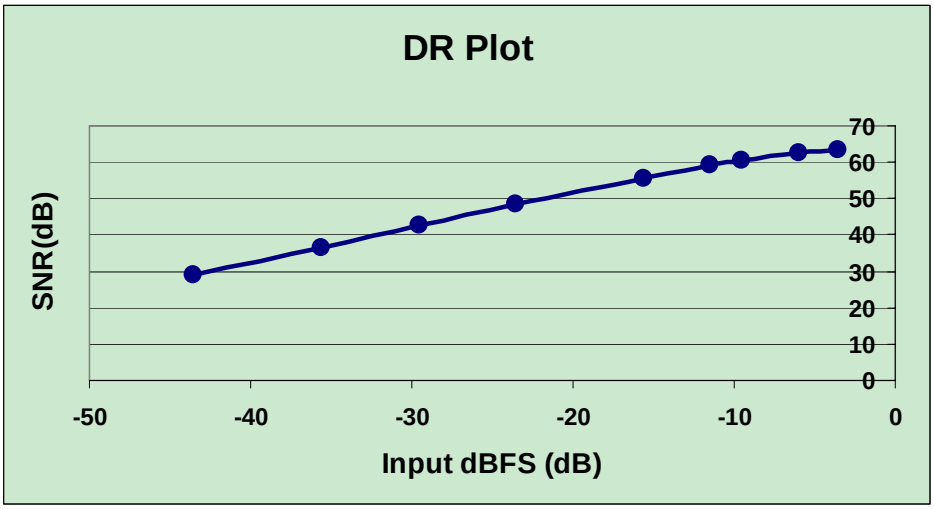


Figure 3.23: Extracted 75 dB DR vs. different input amplitude at 10 Hz bandwidth.

The result of the complete accelerometer system is show below. The sensitivity of the accelerometer is 1.1 V/g. Figure 3.24 shows the output bit stream with an input acceleration at -1 g peak. Figure 3.25 shows the output bit stream with an input acceleration at 0g. Figure 3.26 shows the output bit stream with an input acceleration at 1 g peak. The micrographs of the IC die and the testing board are shown in Figure 3.27 and Figure 3.28, respectively. The IC die size is 3 mm × 3 mm.

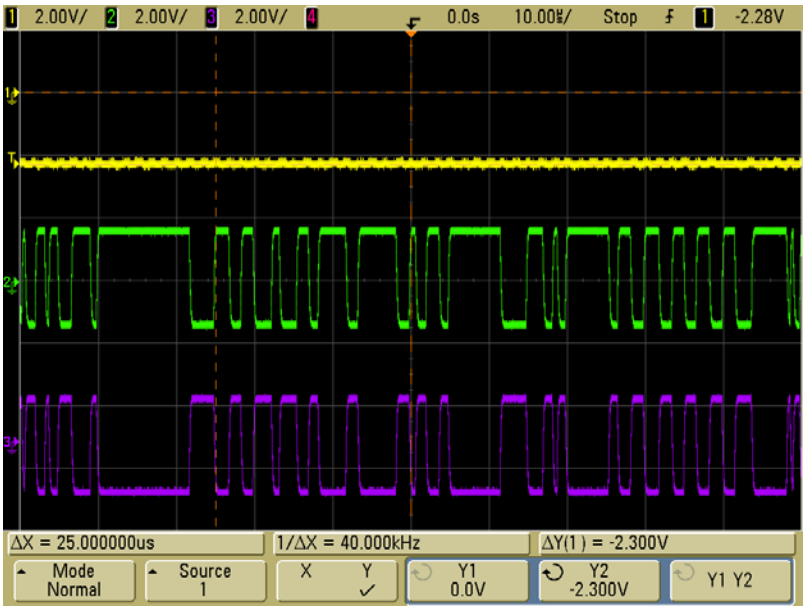


Figure 3.24: The output bit stream at input acceleration at -1g peak.

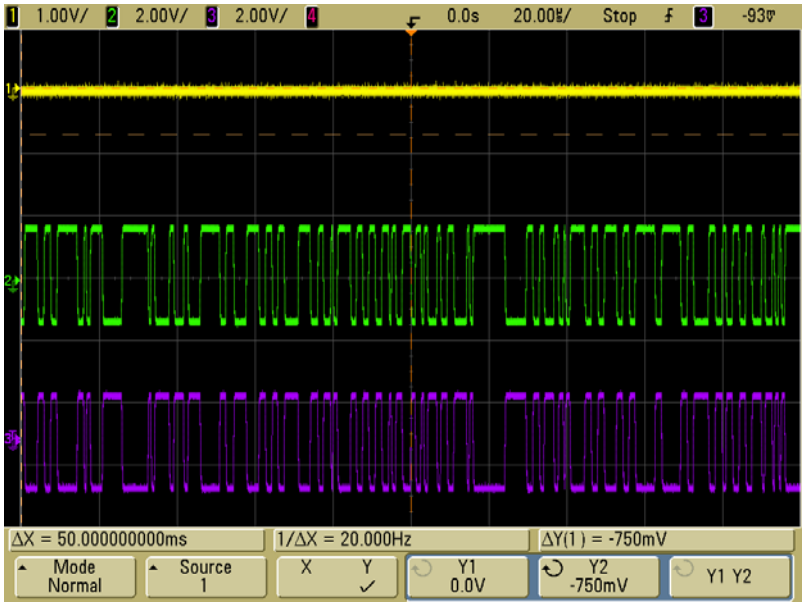


Figure 3.25: The output bit stream at input acceleration at 0g peak.

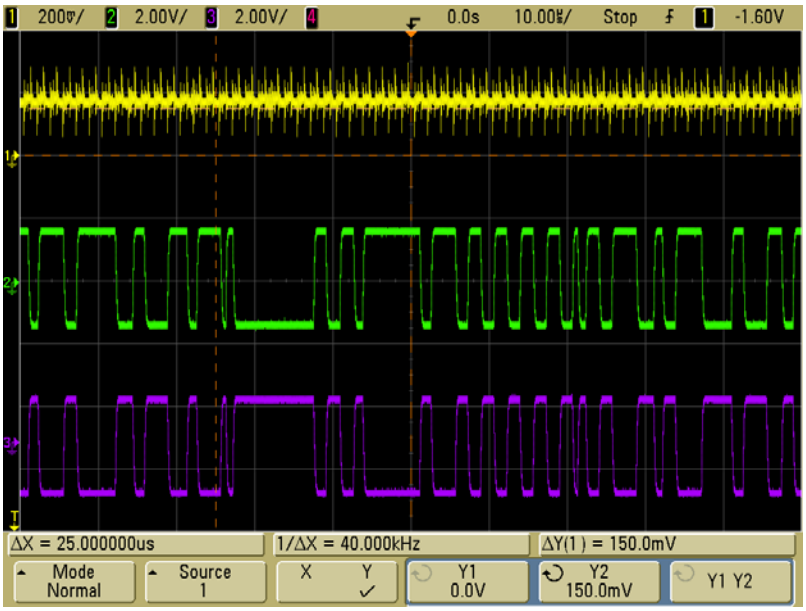


Figure 3.26: The output bit stream at input acceleration at 1g peak.

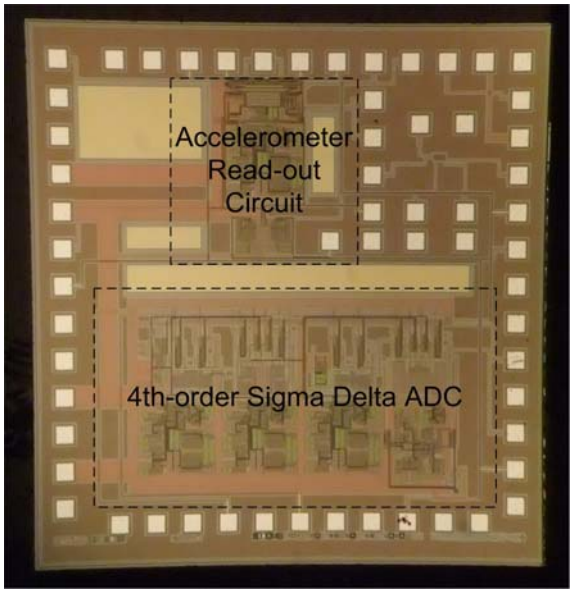


Figure 3.27: The micrograph of the readout + ADC circuit.

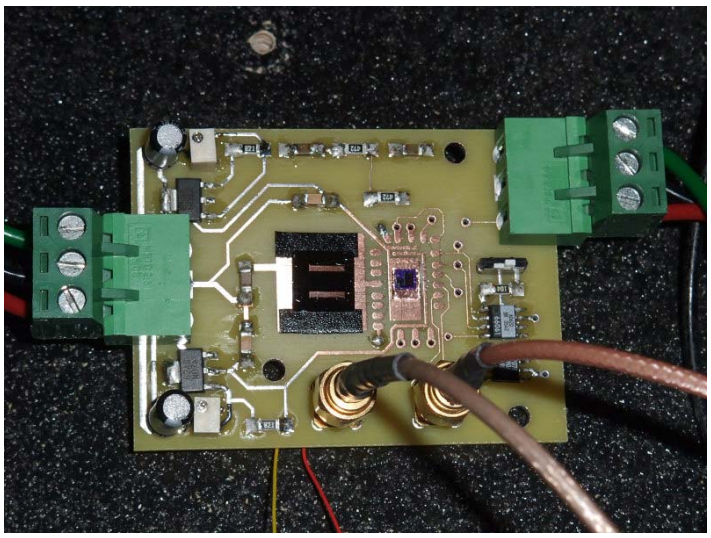


Figure 3.28: The testing board for the accelerometer system.

3.6 Conclusion

This work has investigated design issues in precision accelerometer using an integrated CMOS electrical interface. The interface IC is used to readout a capacitive SOI

accelerometer with micro-g mechanical noise floor. For precise measurement, errors from the electrical interface must be cancelled. The design and implementation of a 3 V fourth-order SC sigma delta modulator in a 0.6μm CMOS technology to attenuate errors including flicker noise, sampling noise, and offset are presented. The SD modulator provides a digital bit stream and has the ability of interfacing with different capacitive sensors with an optimized performance. Very high oversampling ratio (OSR>300) was key to the effective up-conversion of the output quantization noise in a fourth-order SD modulator. The effectiveness of low-frequency noise reduction through chopper stabilization and custom lateral BJT at the inputs of first-stage integrator of the ADC shows a minimum 10dB improvement in noise reduction at near-DC signal frequency range. The measured equivalent dynamic range was 75 dB at 10Hz signal bandwidth, comparing to the work in [5] presenting 85dB DR at 75 Hz signal bandwidth. Results presented in this dissertation suggest technology directions for higher performance accelerometer system. Accelerometer performance is limited by both mechanical and electrical characteristics of the fabrication technology. While the electrical interface presented here attenuates many sources of error, it cannot cancel out all the noise. Integration of capacitive-based inertial sensors with VLSI technology enables increased system functionality. Signal processing and communication capability is desirable for many applications.

CHAPTER 4

CONSLUSION AND FUTURE WORK

4.1 Technical Contributions

In this dissertation, the design, characterization and implementation of micro-gravity MEMS capacitive solid-mass SOI accelerometers with low-power, low-noise, and large DR CMOS interface IC's are investigated. The interface circuit is based on a front-end programmable reference-capacitor-less SC charge amplifier. The accelerometer is fabricated through a dry-release high aspect-ratio reduced-gap process. The following is a list of contributions that have been achieved in this study:

1. The electromechanical design and simulation of the optimized performance capacitive SOI accelerometers is presented. The device sensitivity was improved by reduction of the capacitive gap size through the deposition of a layer of doped LPCVD poly silicon. To obtain deep micro-gravity resolution, the device mechanical noise floor was improved by keeping the thick silicon seismic mass on the backside handle layer of the MEMS SOI die.

   Based on the high aspect-ratio RIE trench etching and backside dry-release, a stiction-less high-yield accelerometer fabrication process that were developed in our group is adopted here. It should be mentioned that a similar fabrication process was developed to implement high resolution micro-gyroscopes in SOI substrates.

2. The implementation and characterization of chopper-stabilized lateral-BJT-input interfaces in CMOS for capacitive accelerometers with micro-gravity resolution and large dynamic range are presented, which includes the custom lateral BJT design and its characterizations. A complete characterization of the noise and power performances was provided for each of the MEMS-IC implementations. The accelerometer system was characterized for the static and dynamic responses. By incorporating the chopper stabilization noise reduction technique in interface circuit, the dynamic range is improved by 10 dB minimum, which leads to a measured resolution of 6.3 μg/√Hz and a dynamic range of 105 dB at 3 Hz. The bias instability was measured at 24 μg for 10 hours with 3.75 mW power consumption for a system fabricated in a 3 V 0.6 μm CMOS AMI process. Also implementation in 0.18 μm TSMC process, it provides compatible performance.

   A remarkable improvement in the noise performances can be achieved by replacing MOSFET's with lateral BJT's in the input differential stage of op-amps. Their good matching, high transconductance and very low 1/f noise make them attractive for use in amplifiers. The full compatibility with conventional, low cost CMOS process suggests competition with BiCMOS approaches for mixed analog/digital applications. Based on the measurements from the IC's made both 0.6 μm and 0.18 μm processes, as long as the base biasing requirement for the lateral BJT's of op-amp is small, even with β variation, it's suitable to integrate them into standard CMOS circuits to achieve extremely low-noise performance at low frequencies.

3. The effectiveness of different noise reduction techniques while they are interfaced with the same accelerometer device is compared and verified. The interface circuits implemented with CDS, chopper stabilization with lateral BJT at input stage, and chopper stabilization with standard PMOS at input stage, are designed and fabricated together in the 0.18 μm TSMC process. The OTA's used in those designs have the identical core design specifications. A minimum10dB improvement in the chopper stabilization scheme in low-frequency noise cancellation is observed by comparing the noise spectrum of the interface systems. Hence 105 dB dynamic range is achieved at low frequency near DC range.
4. In the last part of the dissertation, the design, implementation and characterization of a new monolithic high-order ΣΔ microaccelerometer with micro-gravity resolution and stability and an extended dynamic range of 75 dB at near-DC frequency range is presented. This capacitive architecture that is based on a programmable front-end charge amplifier and back-end fourth-order single-loop one-bit ΣΔ modulator is presented and implemented in a 3V 0.6 μm CMOS technology. In such way, the ΣΔ modulator is effectively decoupled from the sensor to achieve optimized performance regardless of the size of the sensor capacitance. Both function blocks are clocked at the same frequency for power saving and practical implementation. The main idea of applying the sigma-delta modulator concept to a narrowband inertial sensor is to achieve the benefits of the digitization of the accelerometer output without compromising the resolution of the analog front-end. The modulator is realized with fully-differential stray

insensitive switched capacitor integrators to up-convert the quantization noise efficiently at the baseband, suppressing the in-band quantization noise to provide a 1-bit PWM digital output bit stream. The modulator is fully pipelined by realizing all the integrators with one sample delay. This prevents the double-settling problem in which two series connected op amps have to settle in one clock period. When clocked at 600 KHz, the output noise of the prototype sigma-delta modulator achieves 75 dB DR at 10 Hz bandwidth with a resolution bandwidth (RBW) of 1 Hz, while consuming only 4 mW. The measured peak SNDR is 75 dB.

In high resolution $\Sigma\Delta$ modulators, the low-frequency noise such as flicker noise of the op amp may limit the DR. The low-frequency noise can be reduced by the chopper stabilization technique that is implemented in the first stage. Low frequency noise of the MOS device causes undesirable drift and degrades the stability of the data converter. Chopper stabilization with custom lateral BJT implementation at the system level can reduce the circuit noise more efficiently. 20dB improvement in quantization noise and hence large dynamic range is achieved.

A comparison between the presented micro-gravity MEMS capacitive accelerometer system and other state-of-the-art commercial accelerometer systems from Applied MEMS, Inc [96] and Freescale Semiconductor, Inc [97] is provided in Table 4.1. To the best of the author's knowledge, this prototype accelerometer interface is one of the most sensitive capacitive MEMS accelerometer systems that have been reported so far, in

terms of stability, power consumption, low flicker noise, and minimum detectable signal at near-DC-frequency range.

TABLE 4.1: COMPARISON OF SPECIFICATIONS OF MEMS ACCELEROMETER SYSTEMS

Specifications	Out work	Analog Device ADXL103	Colibrys SF1500S.A	Freescale MMA7360L
Full scale (linear output range)	±2 g	± g	±3 g	±1.5 g
Sensitivity	200 mV/g	960 mV/g	1.2 V/g	800 mV/g
Dynamic Range	105dB @ 3Hz	120 dB @ 60Hz	120 dB @ 100Hz	20log(1.5/0.35) @ 400Hz
Power Dissipation	5 mW	3.5 mW	144 mW	1.32 mW
Power Supply	3V	3V – 6V	12V - 30V	2.3V – 3.6V
Technology	0.6μm CMOS 0.18μm CMOS	BiCMOS	N/A	CMOS

4.2 Future Work

4.2.1 Accelerometer Interface Architecture

In this dissertation, the reference-capacitor-less front-end IC is implemented with the ability of interfacing different capacitive accelerometers. The system is single-axis, open-loop, and wire-bonded to the interface chip (two-chip solution to enable independent choice and optimization of process technologies) without wafer-level packaging. Research into a closed-loop interface circuit is therefore a logic next step. Besides this, packaging of the accelerometer system is an important research area and feature for commercialization of one-axis MES-interface open-loop/closed-loop systems, same as for three-axis configurations in many applications.

It is important to measure the acceleration in three dimensions. The potential researches concentrate on the design and implementation of three-axis micro-gravity, large dynamic-range accelerometers in a small form-factor on a single SOI wafer while wire-bonded to a single-unit interface circuit through time-multiplexing scheme. A functional block diagram of such design is shown in Figure 4.1.

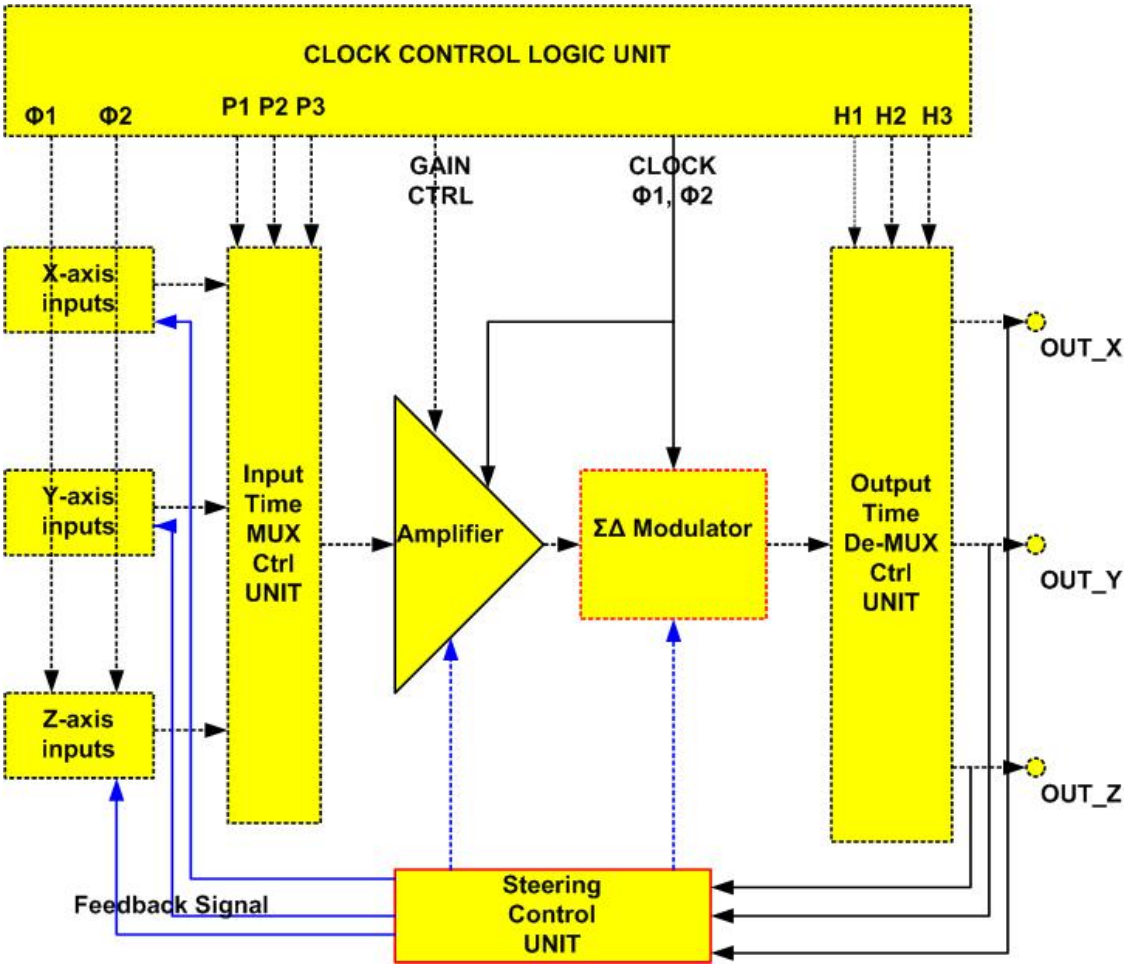


Figure 4.1: Function block diagram of a three-axis accelerometer.

On the other hand, the closed-loop system introduces a phase error. The synchronous demodulation of the output bit stream cannot be performed. The phase compensation filter is introduced to stabilize the loop and to avoid high amplitude limit cycles, which is very important research for the implementation of a closed-loop accelerometer system.

4.2.2 ADC Improvement

The efforts of this thesis are towards the single-bit modulators only. To some levels, recently developed techniques have eliminated the drawbacks of multi-bit ADC modulators. The most significant bit can be used for closed-loop implementation. Therefore, multi-bit modulators have been started to emerge as possible candidates for implementing high-resolution moderate-speed ADC's. A comparison of the single-bit and multi-bit large-dynamic-range voltage modulators, especially in terms of power dissipation might be a good research topic.

To meet the requirement of portable applications, the power dissipation of the prototype modulator can be further reduced without any sacrifice in the performance. In fact, the power dissipation of the second through fourth integrators can be reduced approximately by an additional factor of two by replacing the folded-cascode amplifier with a simple fully-differential amplifier, because the output swing of the integrator with folded-cascode amplifier is less than that of a simple differential pair amplifier. The first stage integrator can be further optimized for lower power consumption by varying the size of the amplification capacitor (C_s). For a given settling time of the amplifier in the first stage integrator, if C_s is increased, the current of the amplifier has to be increased.

On the other hand, if C_s is decreased below a certain value, the current of the second stage has to be increased. Besides, there is another lower limit for C_s is dictated by the input-referred amplifier thermal noise. So any optimization for C_s value which can minimize the power dissipation should be studied.

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